PRACTICAL DECEMBER 1986 · £1.25

ELECTRONICS

SCIENCE & TECHNOLOGY

THE PE PROMENADER
35-CHANNEL DISCO DISPLAY

VIDEO ENHANCER

STEbus IS BACK!

Z80 SINGLE STEPPER

FREE ELECTRONICS CATALOGUE WORTH 70P

DESIGN –
Integrators explained using Op-Amps

TECHNOLOGY –
Making Professional Front Panels

EXPERIMENTATION – *Voice Compression*

PLUS SPECIAL CHRISTMAS BUYERS GUIDE!

THE SCIENCE MAGAZINE FOR SERIOUS ELECTRONICS AND COMPUTER ENTHUSIASTS

CONSTRUCTIONAL PROJECTS

VIDEO ENHANCER by R.A. Penfold 16
A low-cost and relatively simple project for all video enthusiasts which can offer hours of entertainment. There is also a follow up, a video fader, coming next month.

PE PROMENADER by Mike Delaney 28
One of the most versatile disco lights and display programmers available as a hobbyist project. It features stand alone EPROM programmer, 35-channel display and a simple to control playback unit. What's even better – you don't have to be a programming genius or even a computer owner to use it!

VOICE COMPRESSOR by The Prof. 24
This is the latest of our Experimental Electronics projects. It was designed in response to a readers' enquiry about voice compression techniques which do not alter the original tone.

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STEbus IS BACK by Richard Whitlock 38
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There is no need to build brilliant constructional projects only to spoil them by putting them in a 'scrappy box'.

DESIGN-INTEGRATORS 20
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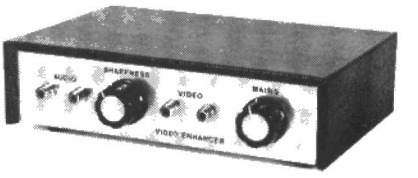
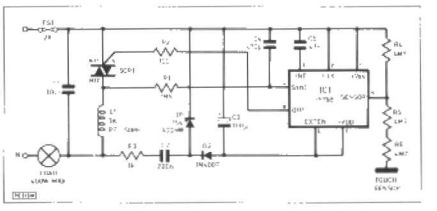
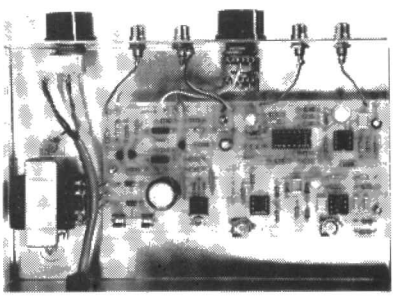
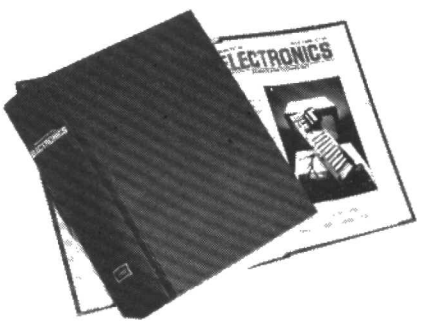
THE LEADING EDGE by Barry Fox 14
In-depth news on the technology behind the technology.

INDUSTRY NOTEBOOK By Nexus 50
Our regular look at the electronics industry. How was Industry Year?



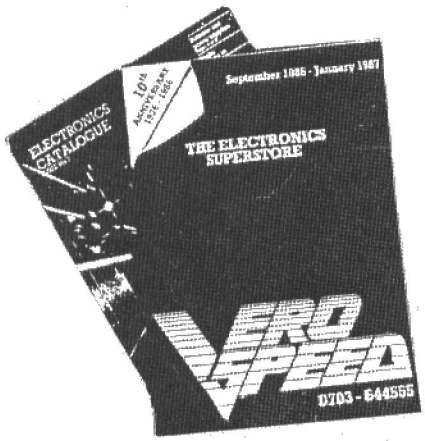






WHAT'S NEW . . .

CATALOGUE CASEBOOK



Over the last month we have received the following catalogues:

The 10th Anniversary edition, Sept 1986 to January 1987, **Electronic Components** catalogue from **Verospeed.** Details from Verospeed, Stanstead Road, Boyatt Wood, Eastleigh, Hants SO5 4ZY.

MS Components Ltd., **Electronics** catalogue. Details from **MS Components,** Zephire House, Waring Street, West Norwood, London SE27 9LH.

The winter catalogue of **Electronic Components** and **Accessories** from **Cirkit** available from selected book stalls, price £1.20. Details from Cirkit Distribution, Park Lane, Broxbourne, Herts EN10 7NQ.

Choosing and **Using Telephones** – advice on the services offered by **BT** available free from OFTEL Press Office, Room E24, Atlantic House, Holborn Viaduct, Lonon EC1N 2HQ.

Comprehensive guide to Flukes range of **digital multimeters** avaiable from **Fluke** (GB) Ltd., Colonial Way, Watford, Herts WD2 4TT.

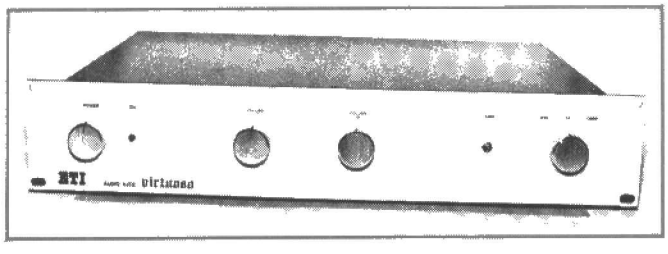
The **Tandy** 1986–87 **Electronics** Catalogue available free of charge from 360 Tandy Stores and authorised dealers throughout the UK.

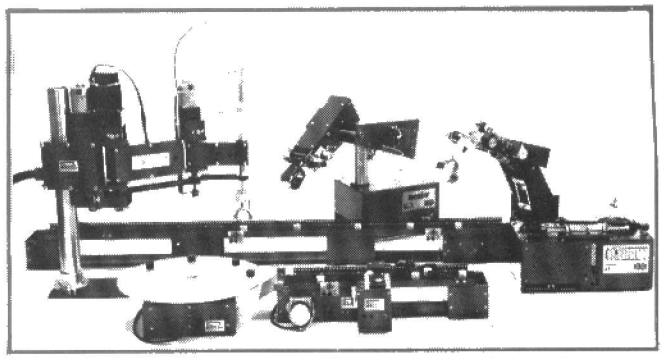
Hi-di-Fi

As most hi-fi enthusiasts will know, the quality of components such as resistors, capacitors, wiring and associated hardware is an important factor in hi-fi equipment design. A noisy resistor in a critical stage in an amplifier, for example, can nullify the effect of spending a lot of money on the rest of the design.

Audiokits, an established hi-fi company, recognise these problems and have taken a fresh look at many existing designs including the Modular Audio Power System published in PE, and are making available a range of kits which include higher grade components which dramatically improve the sound quality of the original design.

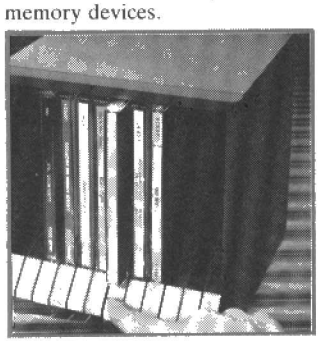
In addition to supplying complete kits, Audiokits are able to supply individual high grade components such as Wondercaps and close tolerance resistors.





Aries Sockets

As the trend towards greater memory size increases it is getting more difficult to find suitable test sockets which can cater for the various sizes of memory i.c.s. Aries electronics have recognised this problem and are now offering test sockets which can accommodate devices up to 32 pins. This is in anticipation of 8Mb EPROM devices which are sure to appear shortly. Aries can offer a complete range of test sockets suitable for all currently available memory devices.



CD Store

A new compact disc storage unit which will conveniently hold 12 discs is available from Earley Marketing Ltd. With a recommended price of around £9.99 it's a little expensive when you consider that CDs can be thrown around, dropped and generally abused with no loss of reproduction quality. However, if you have splashed out on a CD player and are proud of your collection, it might make a nice Christmas present.

It is designed to facilitate an increasing disc collection as it can be clipped to similar units which make up an 'infinite modular system'. The motivation behind the design comes from a need identified by W.H. Smiths and is said to be 'The best British designed compact disk storage unit on the market'. Not interested in CD myself, I would like to see a similar design for computer disc storage at a reasonable price.

Don't be a Wally – Get WALLI!

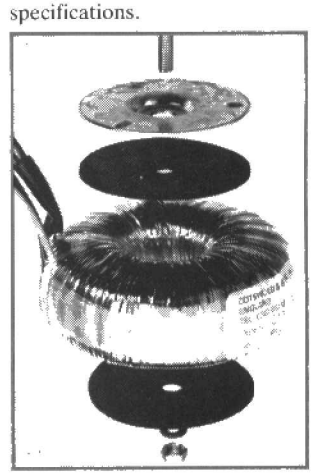
WALLI (Work-cell Amalgamated Logical Linguistic Instructions) is a powerful high level language by which up to four robots and four expansion boards, 'daisy chained' together, may be intelligently operated from a single control computer.

WALLI has been set free by Cybernetic Applications who have produced this simplified language to operate their training robots and auxiliary equipment so that they may simulate a complete production line.

Cybernetic Applications was started by Dick Becker two years ago, during which time he has produced, and is marketing, four robots designed and manufactured by them in Britain. They are the Neptune I and II, Mentor, Naiad and Serpent I and II, all featured in Practical Electronics.

Toroids

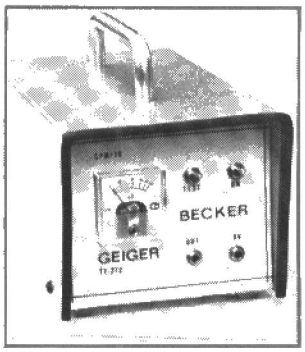
Catering for a special requirement of the German Electronics market has enabled Cotswold Electronics to supply a range of 'budget' toroidal transformers at 15, 25 and 40VA in addition to their standard range. All their transformers in this range conform to various B.S., IEC and VDE specifications.



Geiger

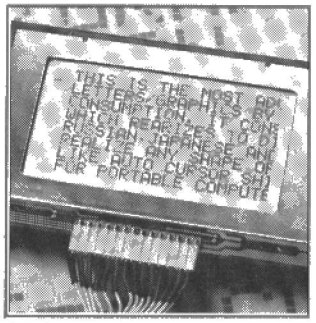
The Geiger Counter project published in August this year has proved to be one of our most popular projects in recent years with interest coming from thousands of readers. John Becker of Phonosonics who designed the project has been innundated with orders for complete kits.

In order to cater for the less experienced hobbyist and the complete novice to constructional projects, Phonosonics now have available a complete range of Geiger counters in both kit form and ready built. Their range includes instruments with panel meters and audible indication with computer interface to almost pocket size meters ready built.



Probe and Pulser

OK Industries are now offering their PRB-50/PLS-500 kit at a special price of £100. The digital logic probe is capable of testing digital circuits from d.c. to beyond 500MHz with a pulse width sensitivity down to 10nS over a range of 3V to 18V

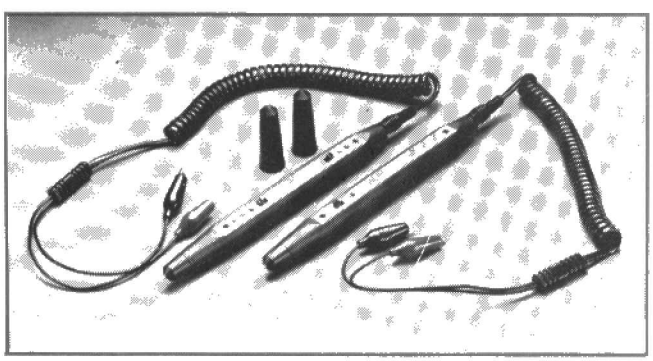


Useful Computer Bits

Earlier this year PE mentioned the M150 mini printer from Epson of which over one million have been sold. Epson have now added to their range of mini peripherals with the introduction of their M185 printer, an addition to the 180 range, and the latest in their mini l.c.d. modules which make a total of seven available.

As the trend towards smaller personal computers and portables is increasing, these products will obviously find their way into numerable designs. With a dedicated processor, a bit of memory and a few control chips and a keyboard, together with a mini printer and display, you have a complete system. At this rate it won't be long before pocket computer systems are available at affordable prices.

Epsons mini display, the EG2201, uses what they call their 'new high contrast ratio super TN technology' which they claim is up to twice as high as that found in conventional large capacity graphic l.c.d.s. and for all practical purposes, 'matches the speed of a CRT and has a life expectancy in excess of 50,000 hours'.



making it useful for both TTL and CMOS circuits. The pulser has switchable options which enable it to inject 100mA signals into circuit nodes of 2uA duration with low repetition rates of 0,5Hz or high repetition rates of 500Hz. It can also drive a node which is not driven by a host circuit or more importantly if the node is under circuit power, it can sense state and voltage and provide the correct voltage at sufficient power to force the node into opposite state.

PSU Range

Verospeed, a well known name to the hobbyist and professional alike, have recently announced a new series of Power supplies which offer a range of features not to be found on many conventional PSUs. They are a family of Thurlby power supplies called the PL range and provide simultaneous voltage and current monitoring on l.e.d. displays with voltage, variable, from 0 to 150% of the rated output and current from 0 to 110%.

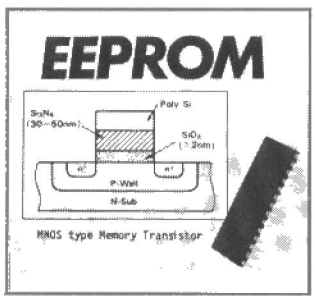
Chips For FAX, Video, Memory and Lasers

This month we have news of several new i.c.s from Hitachi, Intel, Mullard and Mitsubishi, most of them designed for specific or high-tech applications.

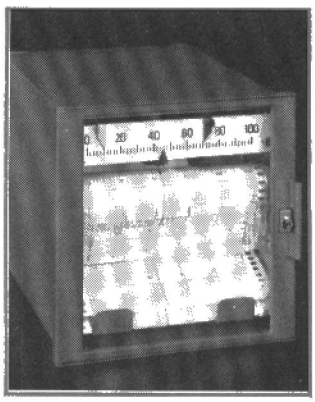
The HM58C65 from Hitachi is a 64K EEPROM organised as 8K X 8 and contains on-chip latches and timer. It has a single rail power supply and power on/off data protection circuitry. Using low power CMOS technology it still manages to maintain excellent speed characteristics.

"first time ever GaAs semiconductor laser with two wave lengths"

Mullard have launched a 256 X 8-bit CMOS EEPROM, the PCB 8582, which has an IC interface which allows a low pin count (8-pin d.i.l.). Power consumption is low and on-chip multiplier provides higher voltages for programming thus enabling the chip to work from a single rail, 5V, supply. A new erasable programmable logic device (EPLD) from Intel, the 5C180, is available from Rapid Silicon. It is a CMOS LSI device which is capable of replacing up to 2,000 equivalent gates of TTL and 74HC SSI/MSI logic. For graphic systems the HM53462 from Hitachi, a dual port DRAM, is designed especially for video applications. Also from Hitachi, a new type of chip is under design, a 'document image compression and expansion processor' (DICEP). Samples are available of the HD63085Y i.c. which is designed for applications in FAX machines, copiers, word processors and telex terminals. It is primarily intended for use in conjunction with their HD63084 DIPP – document image preprocessor which digitalises analogue document image data from an optical sensor. The HD63085Y can compress an A4 document in less than one second.



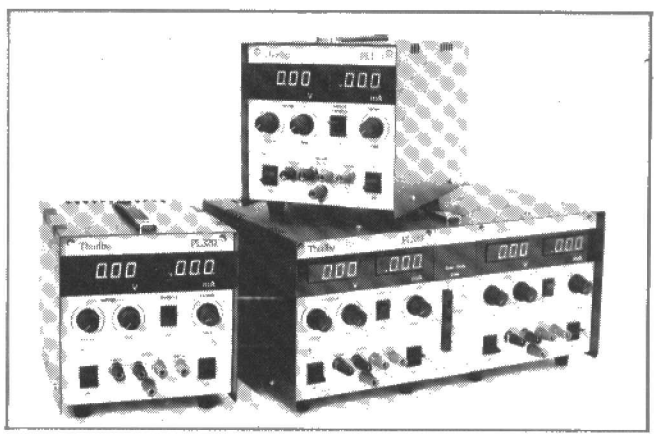
For the first time ever, a gallium arsenide (GaAs) semiconductor laser with two different wavelengths switchable by changing the current, has been developed. Semiconductor lasers are used widely in CD players. The new chip from Mitsubishi allows multiplexed wavelengths for optical communications within a single unit, greatly expanding the traffic capacity.



Case of Recording

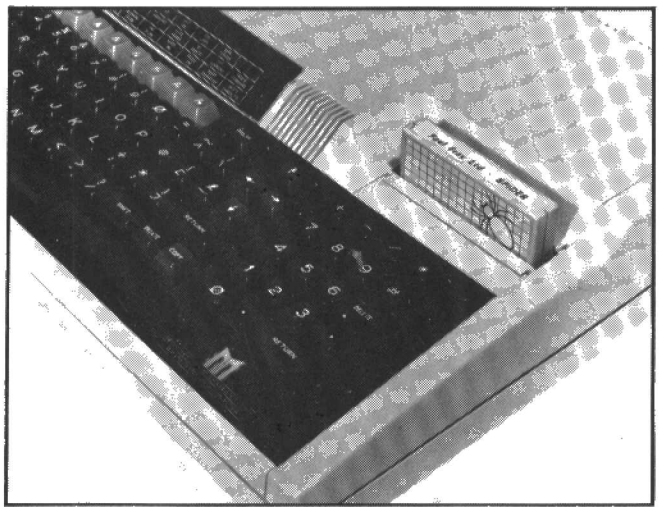
Kent Industrial Measurements Ltd. now have a short case strip chart recorder for around £300 which, they say, is one of the most economically priced single pen recorders on the market.

It requires a panel depth of 186mm and provides fast response, reliability and accuracy from a linear motor pen drive. The input can be derived from a wide range of sensors or transducers producing either d.c. or a.c. voltages or currents over a wide frequency range.



WHAT'S HAPPENING

Trends in personal computing – hardware and software



Computer Add-ons

As most readers of PE own at least one personal computer, it's fitting that we should mention a few computer items in the news pages. Practical Electronics recently had a stand at the PCWshow in London and we were able to assess the general trend in the home micro market.

As expected, the price of more powerful home micros is falling with Amstrad launching an IBM compatible for less than £500. Also as expected in general there are far fewer new computers being launched than in previous years as the buying trend seems to have peaked. However, trade in computer add-ons and software is still going strong with a need for continuing service for existing owners. Next year we will see the price of previously expensive software dropping dramatically, bringing excellent software packages within the range of the amateurs and hobbyists.

Zenith Data Systems are offering a relatively low-cost real time clock system for IBMs, and of course their clones, and Electronic & Computer Warehouse are offering a similar system for Commodore 64s.

As reported earlier this year, in PE, Acorn were working on a reduced instruction set computer and were thought to have a long lead over their competitors. However, Kuma Computers has brought out an RISC processor for the Atari ST which is capable of 7.5 million instructions per second (MIPS). This system can be connected to the ROM port of the Atari ST 68000 based computer providing an extremely cost effective system for advance problem solving previously impossible on a system of this size.

Meanwhile the new BBC Master series of computers seems to be gaining wide ranging approval especially from the education sector. Because of many companies' long term involvement with Beeb compatible products, software and peripheral back-up for the Master series shouldn't be any problem. Paul Fray Ltd., a typical example, has launched a new real time software package, Spider 2, which for the Master series comes in cartridge form and provides real time processing power and allows some degree of parallel processing to be carried out.

Red Boxes

For years now, we have been predicting the arrival of cheap home micros with the ability to provide real-world control functions. Things have been a little slow – most manufacturers have stayed with traditional peripherals such as printers, plotters and monitors etc. Other than a few simple control units and robots, computer add-ons have been left, largely, to electronics magazines such as PE.
Now, however, General Information Systems are supplying attractively packaged intellegent computer add-ons which offer a range of features. The units are called "Red Boxes" and will be described in detail in next months' PE.

FIRM CONTACT

Further details of the products, services and companies mentioned in the News pages of Practical Electronics may be obtained from the following sources:

Cybernetic Applications, Portway Trading Estate, Andover, Hampshire.

Phonosonics, 8 Finucane Drive, Orpington, Kent BR5 4ED.

Verospeed BICC Electronics, Boyatt Wood, Eastleigh, Hants SO5 4ZY.

Audio Kits, 6 Mill Close, Borrowash, Derby, DE7 3GU.

Zenith Data Systems Ltd., St. Johns Court, Easton Street, High Wycombe, Buckinghamshire HP11 1JX.

Paul Fray Ltd., Willowcroft, Histon Road, Cambridge CB4 3JD.

Earley Marketing Ltd., Unit 8, Mercury House, Calleva Park, Aldermaston, Berkshire RG7 4QW.

Epson (UK) Ltd., Dorland House, 388 High Road, Wembley, Middlesex HA9 6UH.

Mitsubishi Electric Corporation, Public Relations Department, 2-3 Marunouchi, 2 Chome, Chiyoda-ku, Tokyo, 100 Japan.

Hitachi Electronic Components (UK), 21 Upton Road, Watford, Hertfordshire WD1 7TP.

NEC Business Systems (Europe) Ltd, Camden Office, 35 Oval Road, London NW1 7EA.

Rediffusion Radio Systems Limited, Newton Road, Crawley, West Sussex RH10 2PY.

Department of Trade and Industry, 1 Victoria Street, London SW1 0ET.

British Telecom, Press and Broadcast Office, British Telecom Centre, Floor A3, 81 Newgate Street, London EC1A 7AJ.

Cirkit Distribution, Park Lane, Broxbourne, Hertfordshire EN10 7NQ.

Fluke (GB) Limited, Colonial Way, Watford, Hertfordshire WD2 4TT.

Rapid, Rapid House, Denmark Street, High Wycombe, Buckinghamshire HP11 2ER.

Aries Electronics (Europe) Ltd., Alfred House, 127 Oatlands Drive, Weybridge, Surrey KT13 9LB.

Cotswold Electronics Ltd., Unit T.1., Kingsville Road, Kingditch Trading Estate, Cheltenham GL51 9NX.

Kent Industrial Measurements Ltd., Howard Road, Eaton Socon, St Neots, Huntingdon, Cambridgeshire PE19 3EU.

OK Industries UK Ltd., Barton Farm Industrial Estate, Chickenhall Lane, Eastleigh, Hants SO5 5RR.

Kuma Computers Ltd., 12 Horseshoe Park, Pangbourne, Berkshire RG8 7JW.

Electronic & Computer Workshop Ltd., 171 Broomfield Road, Chelmsford, Essex CM1 1RY.

WHAT'S TO COME

Telecomms, satellite TV and radio services – looking to the future

The X Factor

For years the British telephone service under both the GPO and BT has been the subject of many a critical and cynical comment, a situation BT is looking to change. The truth is, though, that they provide a first class service bearing in mind they have a network of thousands of miles of cable, thousands of telephone exchanges and millions of telephones to maintain. In recent years the problem has been that with their long term plans to replace all existing exchanges with microprocessor controlled electronic ones, they have been reluctant to invest the necessary time and money on present equipment, much of which is now thirty or so years old. The mere fact that it works at all is amazing when you consider that the bulk of the control and switching equipment is electromechnical – how many washing machines or cars of that age are around now?

Now, however, things are really moving. BT are promising to install, on average, one new digital exchange, every working day. Many, but not all, of the new exchanges will be of the System X type which, because of problems with initial development, are already out-dated in some respects. Nevertheless around 2.5 million digital lines per year will be coming into service offering far more facilities than can be offered using the present system.

By the end of this decade, almost half of all BT customers will be connected to digital exchanges allowing faster call set-up times, better quality of service, and the possibility of a wide range of office automation devices via the IDA. The IDA, Integrated Digital Access, allows modern computer and technology based equipment to originate digital 'calls' and talk to other similarly based machines.

Satellite

Despite its slow start, the satellite receiving equipment industry in the UK seems to be picking up with many more manufacturers and suppliers joining in the fun. NEC and DER have concluded an agreement where DER will distribute the NESAT system through each of their 369 outlets.

By becoming the first major rental company to offer satellite equipment, DER is now one of the largest single sources of satellite receivers in Europe. However, I suspect that will change in the not too distant future.

Rediffusion has launched a range of satellite TV equipment under their Satellite Systems Division. They have gone for a range of discrete products and packages which allow easy installation and a choice of dishes and 'electronic blocks'. Their domestic systems are available in 'carry-home' packs for DIY customers at around £1,000.

Grundig are also producing a satellite package to complement their range of TVs and VCRs. Whilst their receiver is only £399, the complete package will set you back in the region of £1,700.

Personally, I wouldn't advise anybody to rush out and buy satellite equipment in time for Christmas as prices are sure to fall dramatically in the next couple of years or so.

Bids from a number of large companies were placed this year with the government for a share in the UK based satellite industry proposed for the future. Amstrad, a company famous for its value for money consumer electronics products, was amongst the 'bidders'. At the PCW show, earlier this year, an Amstrad employee told me that they are very keen to get into this market and expect to be able to produce a complete package for only a few hundred pounds. One thing is certain, if they do enter the market, competition will certainly get hot.

Radio Control

In order to ensure better radio communications, services and products, the DTI has issued a consultative document outlining proposals for the establishment of a third party quality assurances scheme within the industry.

"give me three good reasons"

Industry Minister, Geoffrey Pattie, said there were three reasons for the establishment of this scheme. The radio industry would gain many benefits from good management practice for quality assurance, there would be reduced need for multiple assessments internationally and regulation of the radio spectrum could, at least in part, be taken away from the DTI.

It is envisaged that if the scheme comes into force, it will apply to manufacturers and importers of radio equipment as well as installers and repairers. In addition some categories of radio users and radio services will be affected.

COUNTDOWN

If you are organising any electrical, computing, electronic, radio or scientific event, big or small, drop us a line. We shall be glad to include it here. Address details to COUNTDOWN, Practical Electronics, 16 Garway Road, Bayswater, London W2 4NH.

PLEASE NOTE: Some of the exhibitions and events mentioned here are trade only or may be restricted to certain visitors. Also please check dates, times and any other relevant details with the organisers before setting out as we cannot guarantee the accuracy of the information presented here.

Instrumentation 87, Feb 25–26, Harrogate Exhibition Centre, March 25–26, Bristol Crest Hotel.
Audio 86, Nov 12–15, Olympia 2.
Drives/Motors/Controls & PC Systems, Nov 25–27, NEC, Birmingham.
Laboratory Manchester 87, April 8–9.
British Electronics Week 87 Olympia, April 28–30.
British Manufacturing Technology Week 87, Olympia, June 2–5.
IEEIE Lectures (various), Oct–Nov 86.

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Editor:
Richard Barron
Personal Assistant:
Karen Poole
Editorial Assistant:
Mary-Ann Hubers
Consultant (Electronics):
R. A. Penfold
Advertisement Sales Manager:
Ian Forbes
Publisher:
Angelo Zgorelec

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Practical Electronics offers a wide range of services to readers including: p.c.b.s, books, subscriptions, back numbers, and software listings. However, due to increased administration costs we can no longer provide photocopies of articles over three years old.

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All editorial correspondence should be addressed to the editor and any letters requiring a reply should be accompanied by a stamped addressed envelope. Please address editorial correspondence to: Practical Electronics, 16 Garway Rd., London W2 4NH. Tel. 01-727 7010
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MY BIT AT THE BEGINNING – 5

Well, that's another publishing year over and now it's time to look towards 1987. However, before I forget, the publishers, staff and myself would like to wish (somewhat early for some) a Happy Christmas to all readers, advertisers and supporters of PE and as they say on the radio, to anyone else who knows us. And for those who think that actions speak louder than words, we are pleased to be able to give away, in conjunction with Greenweld Electronics, an 80-page components catalogue worth 70p. Also, if you make use of our special Christmas order form you can save money on a number of special offers.

It looks as if 1987 is going to be a good year for Practical Electronics as we have a host of excellent constructional projects and features lined up as well as a few surprises.

I hope that you will agree, we are finally getting the balance right, ensuring that there is something of interest to everyone. In response to your demands, we think that together with our regulars, the Experimental Electronics, Design and Technology Features each month offer the best possible editorial profile for a hobbyist magazine. And we are not the only ones who think that!

One of the largest electronic and engineering suppliers in the Middle East has approached us with a view to publishing a Middle East edition of PE. This will take the form of a complete edition of each issue together with additional pages and cover printed in Arabic. This will be available throughout the Middle East from December onwards. It will be distributed to many of their existing customers and sold to most of the universities and teaching establishments.

Whilst continuing to develop PE, we are also launching two new magazines which might be of interest to you. For beginner, experienced or professional astronomers, we are launching "ASTRONOMY NOW", a colour magazine with a wealth of interesting features on all aspects of astronomy, telescope building and astronomical physics. For anyone working at or from home, especially using computers or information technology equipment, we are launching OFFICE AT HOME. Both magazines will be available in early 1987. Keep an eye open for them or fill in an order form to give to your newsagent – or order a subscription for "Spacewatch" at a special introductory price to PE readers using the order form in next month's issue of PE.

MIDDLE EAST PE

A special Middle East edition of Practical Electronics is now being distributed every month throughout the Middle East. It is published under license by Arab Engineers Ltd. See page 62 for details.

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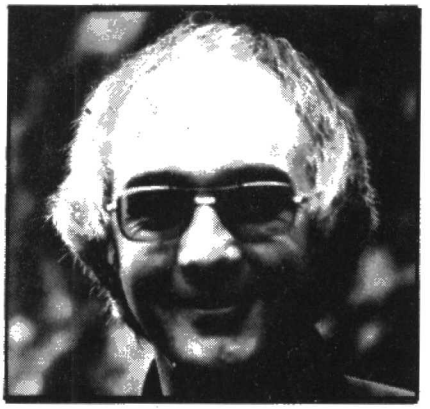


THE LEADING EDGE

REPORT BY BARRY FOX

The technology behind the products

3-D viewing from home video works better in Japan than it does in the UK! The techniques are varied but which system offers the best results? When will we be able to see 3-D VHD Jaws?

BEFORE long the popular press is bound to report that we will soon have 3-D viewing from home video. In September, JVC in Japan started selling a 3-D videodisc system for home use. Earlier in the year Sharp showed the same system to the British trade at a London hotel. Leeds University has developed a similar system for video tape and computer graphics. All these systems work, although not very well. For technical reasons they work better in Japan (and America) than Europe. Here's why.

The Department of Biophysics at Leeds University built a system which displays full colour 3-D pictures on a conventional TV set; the pictures can be derived either direct from a computer or from a pair of video cameras and a videotape recorder. Leeds developed it to study biological macromolecules containing many thousands of atoms. These are so complex that two-dimensional representations are indecipherable. The British army is evaluating the system as a way of displaying a 3-D training film made for tank drivers and gunners.

TECHNIQUE

The technique used is tachistoscopy, or frame sequential stereoscopy. Whereas with cinema 3-D systems the left and right eye images are displayed simultaneously, and viewed separately through coloured or polarising filters, the sequential system displays the images alternately on a TV screen. The viewer watches through a pair of spectacles which alternately shutter the left and right eyes, so that each eye sees only the images intended for it on the screen. The images are recorded in left-right-left sequence on tape, or generated in sequence by a computer.

The difficult part is to synchronise the spectacle shuttering with the sequence of images on screen. The Leeds system does this by superimposing a pair of light spots on the image at the corner of the screen. The spot for the left eye image is in a slightly different position to the spot for the right eye image. A pair of light sensors, stuck to the screen, monitor the spots and produce a series of left and right image switching signals. These are fed down wires to liquid crystal spectacle lenses. When the left light sensor registers a spot on screen, the resultant switching signal shutters the right l.c.d. spectacle lens, and vice-versa.

The system on sale in Japan uses a VHD videodisc instead of video tape or computers. VHD has been sold for several years in Japan as an alternative to Laservision as a carrier for films and music videos. The VHD disc is 26cm in diameter and holds up to an hour of ordinary TV pictures and f.m. analogue stereo sound per side. For 3-D the left and right eye images are recorded on the same disc, one after the other. So the TV screen displays a rapid sequence of left and right eye perspectives. The viewer looks through electrically switched l.c.d. spectacles. The left and right lenses alternately block and transmit light. Switching signals from the video disc player synchronise the system so that the left l.c.d. lens is always closed when the right image is on screen, and the right lens closes when the left image is displayed.

Normally recordings made in this way would be unwatchable on conventional players. Cleverly, JVC capitalises on a disadvantage of its VHD videodisc system to make them compatible. The small, 26cm, VHD disc is able to store a full hour of colour TV and sound information because it records two full pictures for each revolution. This is what makes it difficult for VHD to display clear still pictures. When the readout head is halted or 'locked in the groove' it displays an image on screen which is derived from two still pictures in rapid alteration. If the pictures are not identical, which they won't be if the scene content is moving, the image flutters on screen.

But the two-pictures-per-revolution format provides the ideal carrier for 3-D pictures. One right eye image and one left eye image is recorded for each revolution. When the disc plays on a 3-D player it reads both, and the TV screen displays a rapid sequence of left and right eye perspectives. The synchronised spectacle shutters do the rest. The effect is quite a good depth of image.

When the disc is played on a conventional player of the type sold for several years in Japan, it ignores one image from each revolution. So the image displayed on screen is a single eye 2-D view of the 3-D scene.

THE SNAG

The snag is that, even at the 50Hz picture rate used for Japanese and US TV, each eye sees only 30 images a second. This is too slow to prevent the eye and brain perceiving an irritating flicker. The effect really is very objectionable, and it is even worse on European 50Hz TV, as was clearly seen when computer firm First Class Peripherals of Reading demonstrated a £2000 Leeds system package at a computer show in London earlier this year. Each eye sees only 25 pictures a second and flicker is much more noticeable. The technology may be acceptable for industry and medicine, for teaching students surgery, for instance, but it is surely a non-starter for domestic entertainment; prolonged viewing would be very nasty on the eyes.

It remains to be seen how video buffs in Japan take to 3-D VHD. The first three releases, costing around £40 a disc, are *Jaws 3, Friday 13th Part 3* and *Momoco Club,* described by JVC as featuring 'cute teenage girls'. Seven more similar discs will follow this year.

Although Japanese punters will buy almost anything new because it is new, it is hard to imagine even the Japanese punter regarding 3-D VHD as anything more than a gimmick. Indeed, however clever the technology of VHD, this disc format seems ultimately doomed. Like the ill-fated CED disc from RCA, it relies on contact between the disc and a tracking stylus which reads changes in electrical capacitance. Laservision is an optical system, like compact disc, so there is no wear in use. In Japan, as in the USA, there are now dual optical players – which handle both compact discs and video discs. Sales of VHD and Laservision have been running at around 50/50 until now, but this year VHD's share is dipping. The none-too-cheap and flickering thrill of 3-D is unlikely to stop the rot. PE

VIDEO ENHANCER

BY R.A. PENFOLD

Soft focus or sharpening images

Many people own video recorders and composite video signal monitors and for those who want to improve picture quality this is the project to do it. Please note, though, this project will not work with VHF signals.

VIDEO enhancers vary considerably in their level of sophistication and features, and a basic type is really just a kind of video tone control. By giving a slightly reduced bandwidth a soft focus effect can be obtained, which can be used either for effect, or to combat a high noise level rather like using treble cut in an audio system to counteract record surface noise or tape hiss. High frequency boost gives an effect which is similar to increased contrast, with the impression of increased sharpness, but like treble boost in an audio system, any noise present on the signal tends to be more obvious. In the case of a video signal the noise manifests itself primarily in the form of 'grain'.

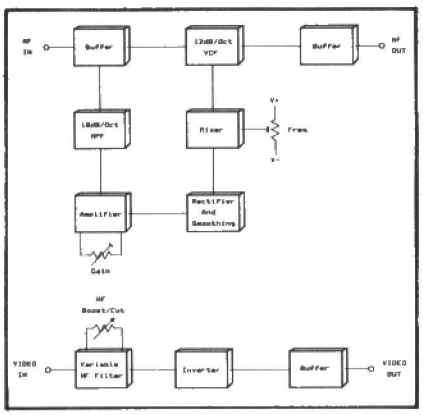


Fig.1. *Block diagram*

Like the tone controls in an audio system, whether the use of boost, or cut, or neither, will give the most satisfactory results depends on the particular signal source in use, the equipment in the system, and the user's personal taste. The enhancer described here has a single control which gives a virtually flat response over the relevant frequency range when it is at a central setting, but which can be backed off to give a reasonably strong soft focus effect, or advanced to give a sharpening effect. The unit is designed to operate with a standard composite video signal (*not* a UHF television signal), and connects between the video output of a recorder and the composite (not RGB) input of a monitor, or in some similar arrangement which provides a suitable signal for processing.

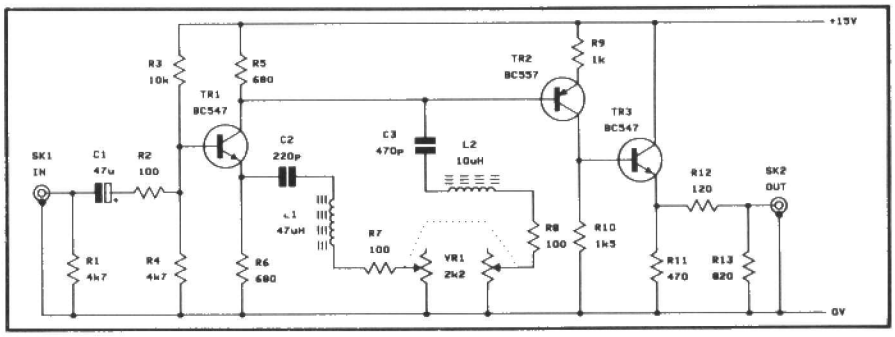


Fig.2. *Video section circuit diagram*

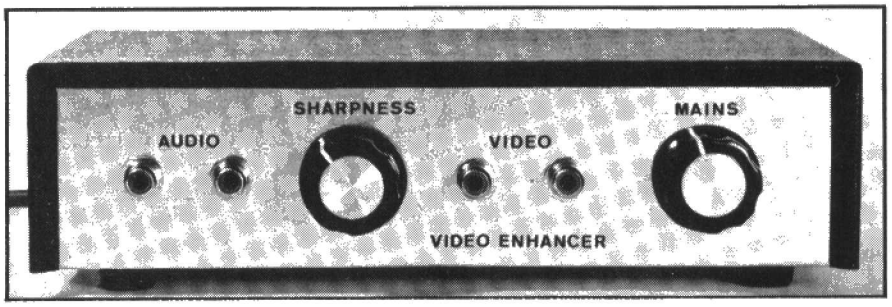
The unit also processes the audio signal, and it provides dynamic noise reduction. This method of noise reduction is excellent for combating high frequency noise such as tape 'hiss', and can give much improved results when applied to the many video recorders which have less than hi-fi audio performance. Dynamic noise reduction is a single ended noise reduction system which only operates during playback, and it will therefore operate with any signal source as no encoding is required at the recording stage.

ENHANCER OPERATION

As will be apparent from the enhancer block diagram of Fig. 1, the video and audio processor stages are completely separate. The video stages are just a simple boost/cut variable filter stage, followed by an inverter which counteracts the inversion which occurs through the filter. Bear in mind that, unlike an audio signal, the polarity of a video signal must be correct, with a positive picture signal and negative synchronisation. The final stage is a buffer amplifier which provides a suitably low output impedance.

The audio processing is rather more complex, and dynamic noise reduction is provided by dynamic lowpass filtering. This could be regarded as a variable treble cut control with the amount of cut provided being automatically adjusted to suit the input signal level. With low input levels the background noise is most noticeable, and maximum treble cut is applied so as to give a large reduction in the 'hiss' level. As the input level is increased, the amount of treble filtering is decreased, until at maximum input there is little or no high frequency roll-off. The point of this is that the signal tends to mask the noise at medium to high signal levels, and the filtering can therefore be reduced without any increase in the noise level becoming apparent.

This system of noise reduction is not perfect in that it does result in a significant loss of treble response at low to medium signal levels but, with no loss of brilliance on loud passages, this is less



obvious than one would expect, and subjectively there is usually a large improvement in the audio quality if dynamic noise reduction is used on noisy signals.

A buffer stage is used at the input of the noise reduction circuit, and the output from this is split between two signal paths. One is the main signal path, and this consists of a second order lowpass (voltage controlled) filter followed by a buffer stage. A 12dB per octave filter offers optimum performance for this application.

The second signal path is the side-chain which generates the control voltage for the filter. The first stage in the side chain is a third order (18dB per octave) highpass filter with a cutoff frequency of approximately 2kHz. It has to be borne in mind here that although loud signals tend to mask the noise, some signals mask it better than others. In particular, high frequency signals mask the noise much better than low frequency ones. Without this filtering there would be a danger of strong bass signals activating the unit and lifting the filtering, but not masking the consequent increase in noise properly. This filter ensures that the unit can only be activated by signals which will fully mask the background noise.

An amplifier boosts the signal by a preset amount prior to rectification and smoothing, to generate a voltage which is roughly proportional to the high frequency input signal level. For the unit to work effectively the attack and decay times of the smoothing circuit must be quite short, otherwise the filter would fail to respond to brief bursts of strong high frequency signal and, of more importance, the filtering would remain lifted for a short while if a strong high frequency signal should suddenly cease. This would result in audible bursts of noise. On the other hand, making the attack and decay times too short would result in very rapid changes in the filter's control voltage, which would produce significant levels of distortion. There is no real difficulty in finding compromise times which give good results in practice, and this is aided here by the highpass filtering which ensures that there are no low to medium frequency signals to smooth out.

The control voltage applied to the filter is obtained by mixing the output of the smoothing circuit with the variable output voltage of a potentiometer. The potentiometer is adjusted to give the required filter cutoff frequency under quiescent conditons, and the gain control is adjusted so that the filtering is only just fully lifted under full input conditions with a reasonably strong high frequency content in the input signal.

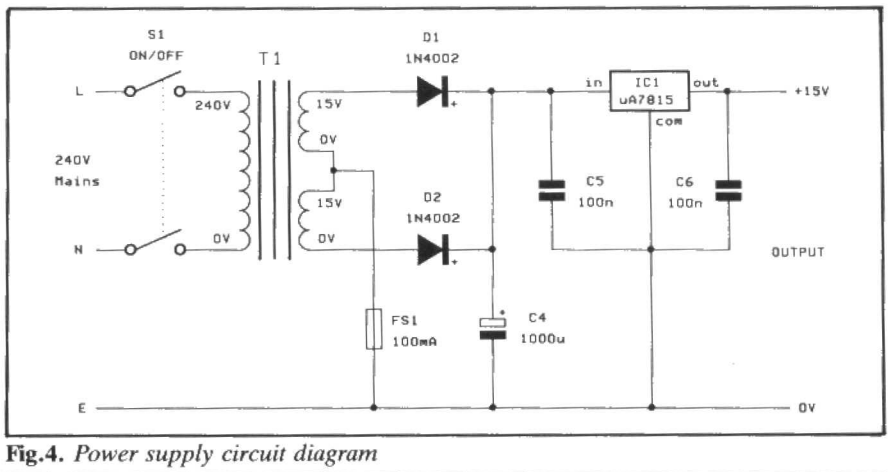


Fig.4. *Power supply circuit diagram*

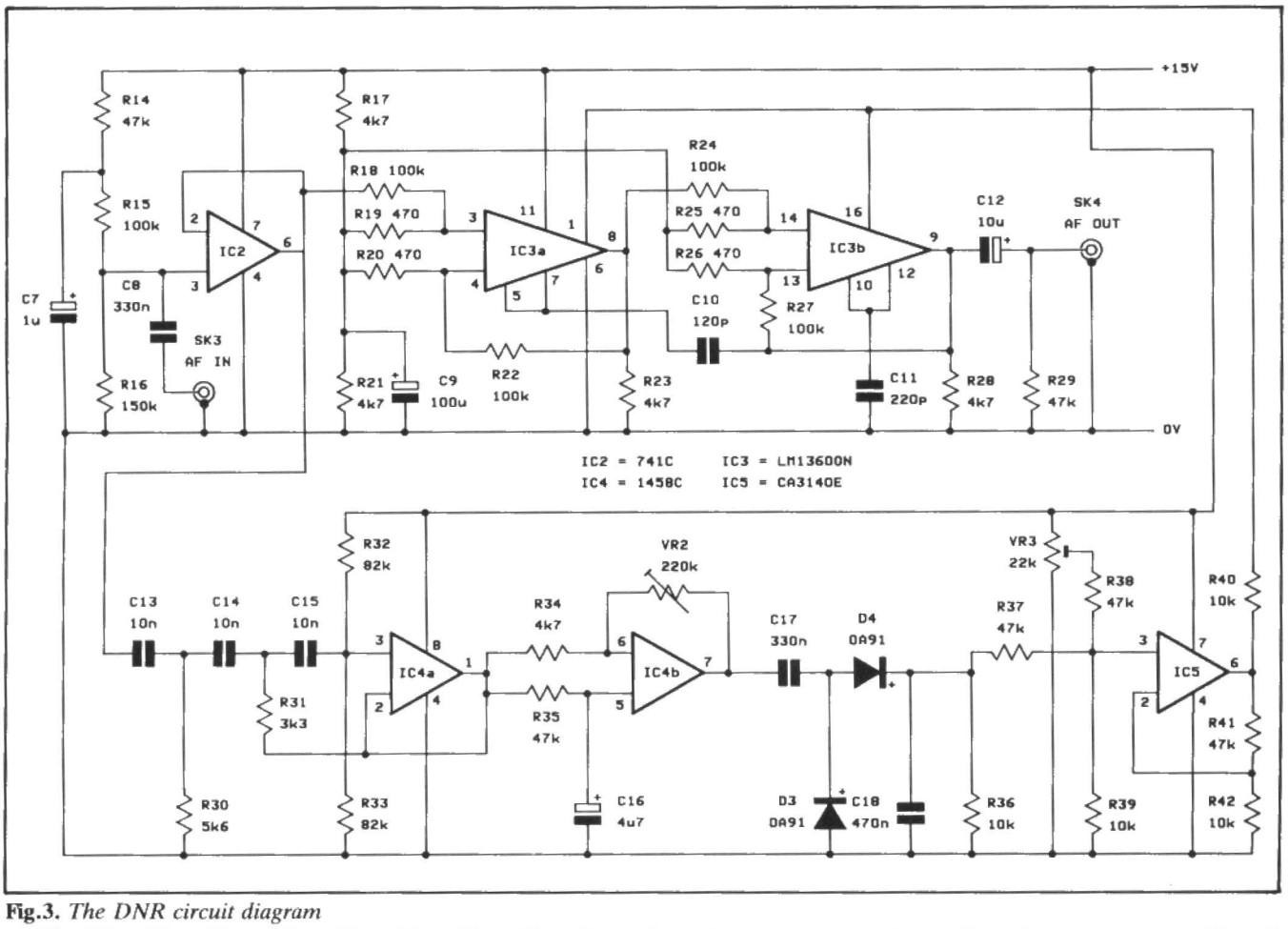


Fig.3. *The DNR circuit diagram*

VIDEO CIRCUIT

Fig. 2 shows the circuit diagram for the video section of the unit. The filter stage is based on TR1 which operates as a common emitter amplifier but, with approximately 100 per cent negative feedback provided by R6, TR1 provides only about unity voltage gain. However, VR1 can be adjusted to bring C2, L1, and R7 in parallel with R6, and it is C2 that is of most importance. This provides a certain amount of high frequency boost by decoupling R6 and removing some of the negative feedback; the amount of boost can be adjusted by means of VR1. The purpose of L1 and R7 is to tame the boost at high frequencies outside the input frequency range, in order to avoid noise and stability problems.

VR1 can also be adjusted to shunt C3, L2, and R8 from the collector of TR1 to earth, and these have the effect of providing high frequency roll-off. It is actually C3 that provides the roll-off and L2 plus R8 simply provide taming of the response. Again, VR1 can be adjusted to vary the amount of filtering. Of course, the two sections of VR1 are used in antiphase, so that the high frequency cut is provided at one end of its adjustment range, with the high frequency boost being provided at the other end. Ideally a centre tapped potentiometer would be used in this application, but suitable components do not seem to be available from retail outlets, and a slightly revamped arrangement with a dual gang type has to be utilized instead. The only slight drawback of this method is that adjustment over the middle part of VR1's range has little effect, with most of the boost and cut being introduced well towards the extremes of its adjustment range.

TR2 is a second common emitter amplifier and it acts as the inverter to restore the signal to the correct polarity. TR3 is an emitter follower buffer stage, and the output signal is tapped off from the emitter of TR3 via R12 and R13.

DNR CIRCUIT

The full circuit of the dynamic noise reduction unit appears in Fig. 3. IC2 is a straightforward unity gain buffer stage at the input, and the voltage controlled filter is based on IC3. This is an LM13600N (or the almost identical LM13700N) dual transconductance operational amplifier. Both amplifiers have emitter follower Darlington pair output stages, and these have R23 and R28 as their discrete load resistors. The buffer in IC3b serves to provide the unit with a low output impedance without the need for a separate buffer at the output. The filter is a two stage Butterworth type.

IC4a acts as the buffer amplifier in the highpass filter, and this is a conventional three pole active design. IC4b acts as the amplifier stage. The gain of this inverting mode circuit can be adjusted by means of VR2 from zero at minimum resistance to around 54dB (470 times) at maximum resistance. This enables the circuit to work well with a maximum input level of anything between a few tens of millivolts and a few volts peak to peak.

The output of IC4b is rectified and smoothed by a conventional halfwave circuit based on germanium diodes D3 and D4. The output of the smoothing circuit is mixed with the output of VR3 by what is really a passive mixer followed by a voltage amplifier (IC5), rather than a true active mixer. The filter is current rather than voltage controlled, but R40 is added in series with the control input of the filter so that the current flow is roughly proportional to the output voltage of IC5, and the filter is effectively converted from current to voltage control.

COMPONENTS . . .

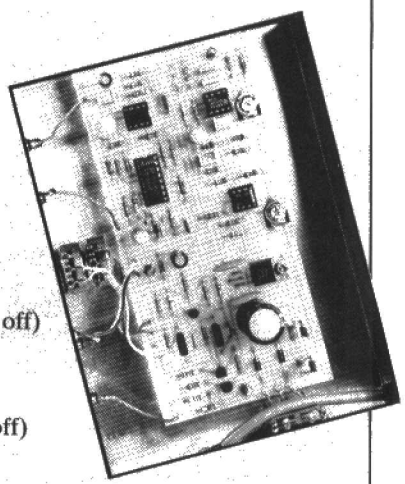
VIDEO ENHANCER

RESISTORS

R1, R4, R17, R21, R23, R28, R34	4k7 (7 off)
R2, R7, R8	100 (3 off)
R3, R36, R39, R40, R42	10k (5 off)
R5, R6	680 (2 off)
R9	1k
R10	1k5
R11, R19, R20, R25, R26	470 (5 off)
R12	120
R13	820
R14, R29, R35, R37, R38, R41	47k (6 off)
R15, R18, R22, R24, R27	100k (5 off)
R16	150k
R30	5k6
R31	3k3
R32, R33	82k (2 off)

POTENTIOMETERS

VR1	2k2 1in dual gang
VR2	220k sub-min hor. preset
VR3	22k hor. sub-min preset



CAPACITORS

C1	47μ 25V radial elect
C2, C11	220p ceramic (2 off)
C3	470p ceramic
C4	1000μ 25V radial elect
C5, C6	100n ceramic (2 off)
C7	1μ 63V radial elect
C8, C17	330n miniature polyester (2 off)
C9	100μ 16V radial elect
C10	120p ceramic
C12	10μ 25V radial elect
C13, C14, C15	10n miniature polyester (3 off)
C16	4μ7 63V radial elect
C18	470n miniature polyester

SEMICONDUCTORS

D1, 2	1N4002 (2 off)
D3, 4	OA91 (2 off)
TR1, TR3	BC547 (2 off)
TR2	BC557
IC1	μA7815
IC2	741C
IC3	LM13600N or LM13700N
IC4	1458C
IC5	CA3140E

MISCELLANEOUS

SK1, SK2, SK3, SK4 chassis mounting phono (4 off); S1 rotary mains; FS1 20mm 100mA antisurge; T1 mains primary, twin 15V 100mA secondaries; L1 47μH RF choke; L2 10μH RF choke; case about 203 × 127 × 51mm; control knob (2 off); printed circuit board; pair of fuseclips; 8 pin DIL i.c. holder (3 off); 16 pin DIL i.c. holder; Mains lead and plug, pins, wire, etc.

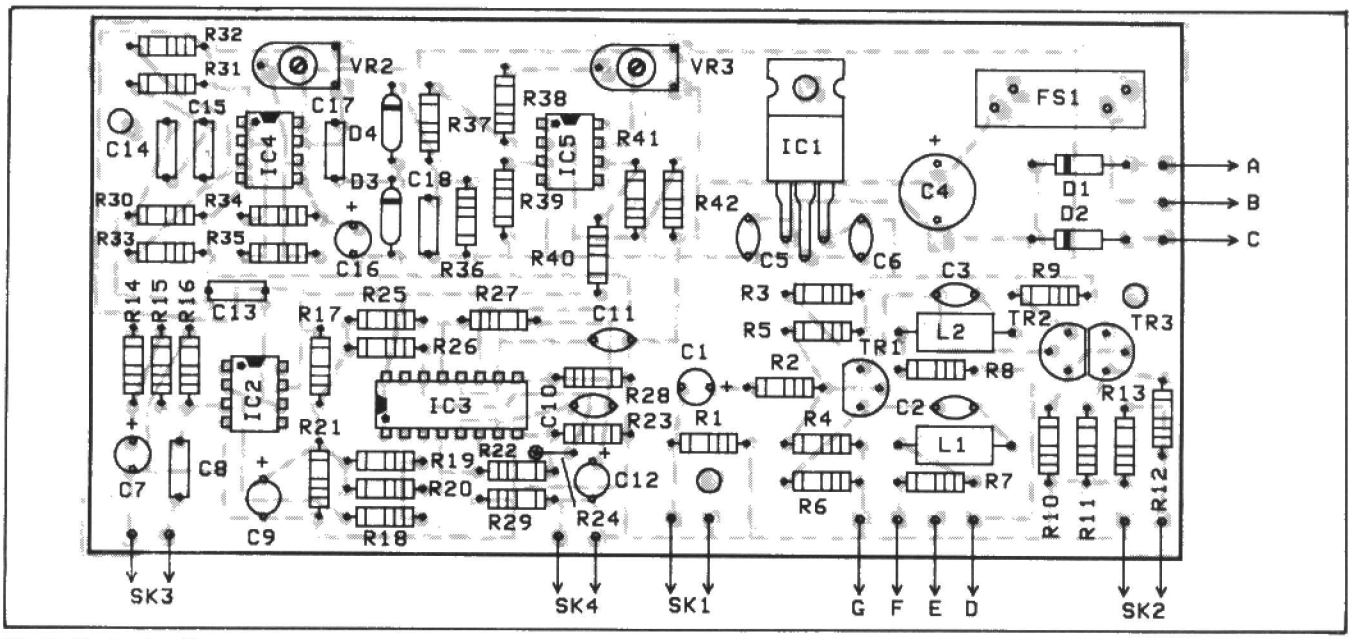


Fig.5. *P.c.b. details*

POWER SUPPLY

There is nothing out of the ordinary about the mains power supply circuit (Fig. 4). This uses a mains transformer which has twin 15 volt secondary windings connected to effectively give a 15-0-15 volt winding to drive a push-pull type rectifier circuit. C4 provides a large amount of smoothing, with IC1 then providing regulation and electronic smoothing so that a low ripple and well stabilised +5 volt output is provided.

CONSTRUCTION

Construction is simplified by having practically all the components on a single printed circuit board, and details of the board are provided in Fig. 5.

As IC5 has a PMOS input stage it should be fitted in a socket and the other standard antistatic handling precautions should be observed when dealing with this device. Fuse FS1 is mounted on the board in a pair of fuseclips. Make sure that these are fully pushed down onto the board before soldering them in place. It is preferable to use an antisurge fuse rather than the more common quick-blow type as the latter would tend to blow at switch-on due to the large surge current as C4 charges up. IC1 does not require a heatsink, but it is a good idea to mount it horizontally and to bolt it down to the board so that it is firmly held in place without putting any undue stress on the pads. D3 and D4 are germanium diodes which are much more vulnerable to heat damage than the more familiar silicon types. Due care should therefore be exercised when fitting these two components, and the bit should be applied to the joints for no longer than is really necessary. Pins are fitted to the board at all the points where connections to off-board components will eventualy be made.

Little hard-wiring is required in order to complete the unit. It is not essential to use screened leads to connect the sockets to the board, but these leads

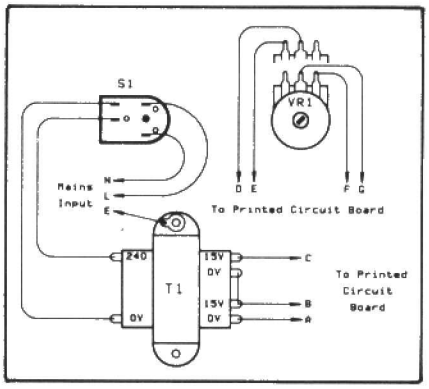


Fig.6. *Wiring details*

should be kept short and direct. SK1 to SK4 are all phono sockets on the prototype, but these can obviously be changed to other types if these would better suit the equipment with which the unit will be used. The other point to point style wiring is illustrated in Fig. 6 in conjunction with Fig. 5 (e.g. point 'A' in Fig. 5 connects to point 'A' in Fig. 6). Although the power supply wiring is very simple, check the finished unit very carefully paying particular attention to this aspect of construction as any errors here would be potentially disastrous.

ADJUSTMENT

No adjustment is required to the video processing circuit, and the effect of the enhancer control will be immediately evident on most program sources, although the unit will have little effect on a very dull and low contrast picture. Adjustment of VR1 in an anticlockwise direction gives the soft focus effect, while setting it in the opposite direction gives the outline sharpening effect. The degree of control provided by the unit can be increased by raising the values of C2 and C3, but in practice the specified values give what is really about the maximum usable degree of boost and cut. There should be no significant change in brightness or contrast with the unit added into the system and VR1 adjusted to a mid-setting.

If suitable test gear is available, VR3 can be set for the desired filter cutoff frequency (with VR2 set for minimum gain so as to prevent the unit from responding to the test signal). VR2 is then advanced to a point where a strong high frequency signal just about fully lifts the filtering (i.e. raises the cutoff frequency to around 15 to 20kHZ).

It is perfectly possible to set up the unit correctly without the aid of any test equipment, and this possibly represents the best way of doing things. With VR2 set for zero gain, VR3 is adjusted to give the required degree of noise reduction. Avoid the temptation to set the cutoff frequency too low as, although it will give an impressive amount of noise reduction, this would result in the action of the unit becoming clearly audible in use. VR2 is then advanced as far as possible without an increase in noise becoming apparent on medium strength signals. It is really a matter of using a little trial and error with a program source that has a wide dynamic range.

As described here the unit only provides monophonic audio processing, but for stereo operation it would merely be necessary to build up a second printed circuit board to handle the second channel (omitting the power supply and video circuits of course). The power supply is easily capable of supplying the additional current required by an extra DNR circuit. It would probably be necessary to resort to a slightly larger case though. PE

SUCCESSFUL INTEGRATORS –THEORY AND PRACTICE

BY PAUL CUTHBERTSON

An op-amp design course

Integrators are used in a host of circuits, to generate wave forms, in filters, in measurement applications and in analog computers. They are a source of much wailing and gnashing of teeth, when they do not work as we would like; this article sets out to point out the major pitfalls, and outlines the operation of integrators, going on to comment on component selection and to describe a practical, high performance circuit. Many of the topics discussed apply to designing with op-amps in general.

A PERFECT integrator's output voltage will ramp according to the size and direction of the current flowing into it. Fig 1 shows the general circuit for an integrator, and the behaviour of the output voltage with various input currents flowing.

The current flows into the capacitor, charging it, and since the op-amp attempts to keep its two inputs at the same voltage, the output has to ramp to keep pace with the charging. The inverting input of the op-amp is a virtual earth. We have to assume that no current flows into the input of the op-amp; this is an important point and is mentioned in greater detail later. Incidentally I have chosen to regard a current flowing into the integrator as positive. Zero volts is defined as being half way between the power supply rails, this being the usual case. These comments apply to the ideal integrator, which does not exist, but which will serve to illustrate the principle.

INPUT RESISTOR

Fig 2 shows how we can generate the current from an input voltage via a simple resistor. The circuit probably looks a bit more familiar now. Since the inverting input is held at zero volts, we can easily work out that the input current is Vin/R. This input current charges the capacitor in just the same way as before, the output voltage going negative as current flows into the integrator.

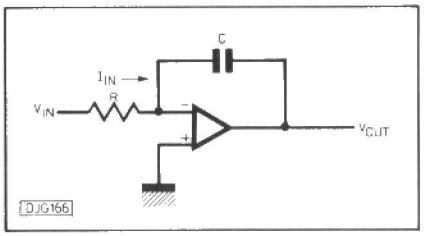


Fig.2. *How can you resist it?*

SUMMING JUNCTION

Fig 3 shows how we can add on further resistors to make a summing junction. The input currents are summed at the inverting input of the op-amp, which is still held at zero volts, so we can work out the currents for each resistor separately and add them to get the total current. We must pay attention to the polarity of the current; if we have a current flowing away from the junction, it is negative and adding it in will send the total more negative.

To take an example, assume that the input resistors are all equal at 1M. If we have three input voltages of one volt, two volts, and minus four volts, then the net current will be minus one μA, and the integrator output will ramp positive. To be more poetic, all the current 'supplied' by the positive inputs has been 'drained away' by the negative input, and then some. Furthermore, if we imagine that one of the input resistors is connected to zero volts or left open, then its contribution to the input currents is nothing.

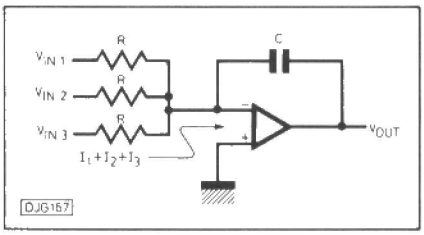


Fig.3. *Some thing is happening!*

CAPACITOR VALUE

At this stage it would be useful to be able to work out how fast the integrator output will ramp, for a particular size of capacitor. We can use the equation CV = it if we wish to invoke currents, but since i = V/R, we can simplify this to C = t/R and rearrange it to make any of capacitance, resistance or time the subject on the left hand side. t = CR is one way of rearranging it – now does that look familiar? It's the relationship for time constant. In this context, it means that the integrator capacitor C will charge through the same magnitude as the input voltage (but in the opposite direction of course) in CR seconds.

If the output starts at zero volts, and our R and C are 1uF and 1M, and we

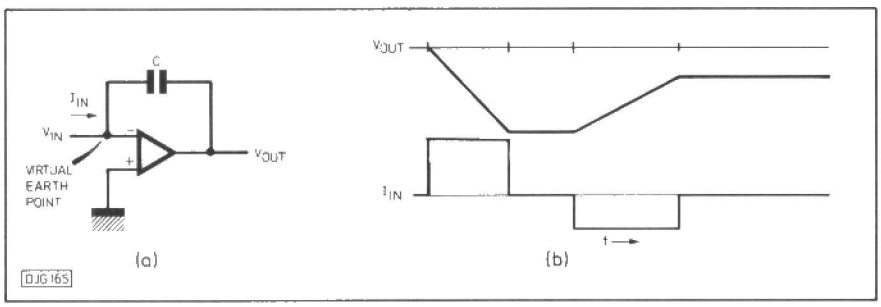


Fig.1. *Basic principles.*

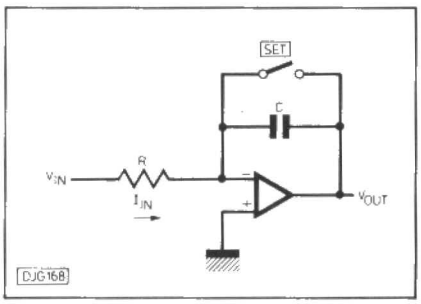


Fig.4. *Set circuit.*

apply ten volts to the input, the output will ramp through ten volts, (to minus ten volts) in one second. This integrator has a time constant of 1s and a bandwidth of 1Hz. To expand the equation to include the input and output voltages, we get Vout =– Vin t/RC where Vout is the change in output voltage from the initial condition, and the minus sign accounts for ramping in the opposite direction to the input voltage. We are assuming that the input voltage remains steady over the period of interest.

What happens with a varying input voltage is quite interesting, but we cannot go into that here.

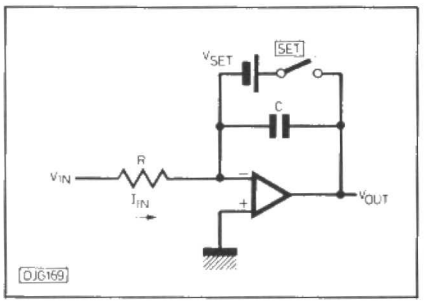


Fig.5 *A game set.*

SETTING AND HOLDING

When the integrator is part of a computation or measurement circuit, the ability to set an initial condition, and to hold the integrator at any time (i.e. to get it to ignore the inputs), is mandatory. Similar principles might apply to filters and waveform generators whose ranges we wish to switch, or to waveform generators which must be reset every cycle, say to generate saw tooths (or saw teeth?). Without discussing the exact nature of any switches just yet, we can take a look at where they must go in the circuit.

Discharging the capacitor is quite simple; see Fig 4. A switch is connected across the capacitor, which shorts the capacitor when closed, discharging it and setting an initial condition of zero volts. It is more likely that we want to set some initial non zero condition. Fig 5 shows the usual text book circuit, which connects a battery or other voltage source across the capacitor, charging it to that voltage with the switch closed. This is all right in so far as it goes, but practically we may want to set a number of integrators at once, to a variety of different voltages. We cannot use the same voltage source for all our integrators, unless we switch both sides of it (if we didn't, the integrators would be connected together permanently at some point and their operation would be deranged). It seems that we have to have a number of two pole switches, and set each integrator individually, or as many floating voltage sources as there are integrators.

This is one of the class of problems known to engineers as the 'lets add another bit on's. The extra bit we add in this case is another op-amp plus a few resistors. Fig 6 shows how we can get away with the simple shorting switch to discharge the capacitor, and add in the Vset at the second stage. Notice that the two op-amp circuit no longer inverts, although an analog computer user would require it to. We can have gains other than one in the second stage if we wish. More on this score in the practical circuit below.

To hold the integrator, let us simply interrupt the input current, so that it can no longer charge the capacitor. Fig 7 shows a switch in the ideal position. Individual switches could go next to the input terminals, (for range switching perhaps) but see below for comments regarding CMOS analog transmission gates.

CHOOSING A CAPACITOR

To begin with the least complex of the decisions a designer of integrators is faced with, we should take a look at the capacitor. Calculating a capacitor value is discussed above. If we end up needing a monstrous value, we should consider increasing the input resistance, and if we are after huge time constants, of the order of hundreds of seconds, then it may even be worth going digital; but there is no space to discuss that aspect here. Another trick to increase the apparent time constant is to attenuate the input voltage. Really large, close tolerance capacitors such as a 10μ 5% polycarbonate can cost us a fiver a shot, and are reserved for the wealthy!

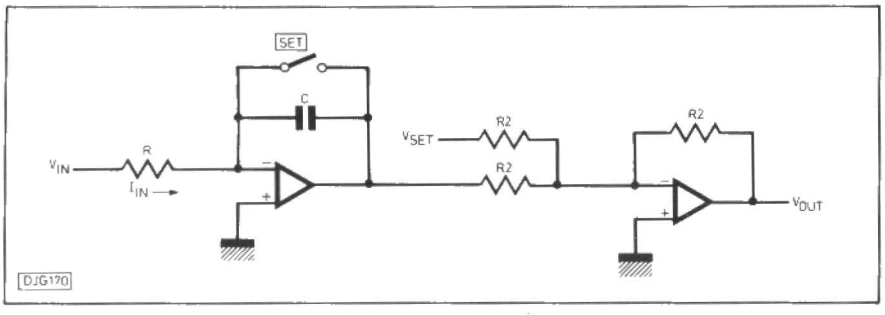


Fig.6. *Game, set and match.*

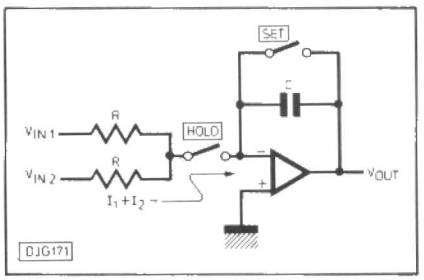


Fig.7. *This is a hold up.*

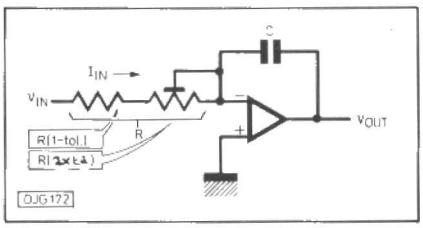


Fig.8. *Trimming her up (Not sexist).*

As far as types are concerned, let us not be tempted to use electrolytics. They have a high leakage current, a poorly specified capacitance value, they are polarised, and (less important) have a high equivalent series resistance and inductance. Any of these failings is enough to tell us to leave them alone.

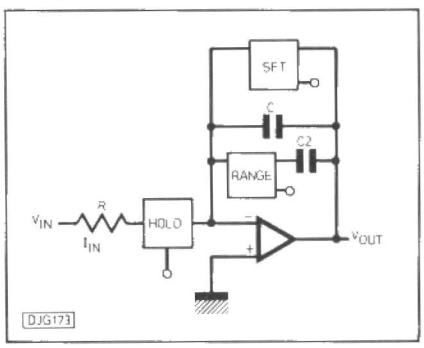


Fig.9. *Transmission gates to the rescue.*

For integrators used in computation, measurement and waveform generation, we need stability and low leakage currents. For values up to about 10nF, polystyrene types have excellent low leakage characteristics, and silver mica better temperature stability than most, and both are available in 1% or 2% tolerances quite cheaply.

For values greater than 10n polyester is a reasonable choice, even for computation purposes, if we are not to get expensive. We can trim out the larger initial tolerance. Polycarbonate has a better temperature stability than polyester, and is available in uF sizes. A stable, close tolerance ceramic in a high value is expensive.

CHOOSING A RESISTOR

Metal film resistors have a closer tolerance and better temperature coefficient than high stability carbon types, and are preferred for critical positions, such as the input resistors on computer integrators. It is hardly worth using anything less good than a carbon histab, they are virtually as cheap as anything less. For filters, generally speaking, we are less concerned with precision, but for other purposes it is good to be able to trim out the variations in time constant, due to resistor and capacitor tolerances. Fig 8 shows a fixed and a variable resistor in series for adjustment; we can get quite 'close in' with the fixed resistor, and use the pot to trim the rest of the way, avoiding a very coarse, difficult adjustment.

To choose values of fixed and variable resistor, first choose a value of fixed resistor that is smaller than the calculated value by about the tolerance of the capacitor or greater. Then choose a variable resistor twice the difference between the chosen fixed resistor value and the calculated value. To give an example, say the capacitor tolerance is +/− 10% and R needs to be 1M. We might choose the fixed resistor to be 910k and the variable resistor to be 200k. This might be a bit tight if the capacitor value really is 10% out; although it makes for a nice fine adjustment. It may be better to choose a fixed resistor of 820k, and a variable resistor of 500k, which gives a wider, but coarser, adjustment.

Carbon skeleton pots are very cheap and quite adequate for trimming out the worst excesses of a filter, perhaps of the Chebyshev shape which is more sensitive to component tolerance than the more lenient Bessels and Butterworths. Multiturn cermet trimmers are the best thing for high performance, having a better temperature coefficient and a finer adjustment. Any potentiometer will degrade the performance of the circuit with temperature.

If this is very important, or if your pocket is more important than your time, (if you're like me you'll have difficulty making up your mind on that one!) consider selecting two fixed resistors to put in series to make up the required value. It is easier to use series resistors than parallel, and the result is likely to be just as close to the value you want. This method is not amenable to quick adjustment! A decade box is handy if you are going to select resistors. Metal film resistors are often available in the E24 values, getting closer to the value you ultimately need.

SWITCH SELECTION

Having dispensed with the passive side of things, there are two items left; the switches, if needed, whether mechanical or electronic, and the op-amp itself.

Taking the switches first, we could choose panel switches, relays, or CMOS transmission gates. At the simplest, we can have a push button on the front panel, and two wires trailing to the circuit board. This is all right until we consider that a single button will only work one integrator, and that the wiring, which is carrying tiny currents, can pick up interference very easily. The integrating action might end to 'smooth out' at pickup, but even so! Let's avoid the situation if at all possible.

A better solution is to use reed relays, where one panel mounted control can work many circuits, and the conductors carrying our precious signals can all be safely left on the board. However, relays can be expensive and they suffer from bounce. If we have a computer integrator, which we run for a millisecond at a time and them sample, we don't want a hold relay clattering up and down for five or six times that, not on your life. Add to this the power consumption of the coils, the drive requirements, electromagnetic noise, temperature variations, and the rest, and we can end up in a pickle with more than a few relays.

The analog transmission gate to the rescue. They use very little power, are quiet in use and do not suffer from bounce. They are easy to drive too. The types most commonly seen are the 4016/4066 kind, or the 4051 multiplexor or similar for range switching and the like. The 4066 and 4016 are pin compatible, the 4066 being the improved version with a lower and more consistent 'on' resistance. (Does anyone still buy 4016's?)

Their drawbacks are that, like most semiconductors of our acquaintance, they are easily damaged; and their 'on' resistance, rather than the few milliohms of a relay, are some tens of ohms typically. However with a little consideration we can get round these inconveniences and the results are excellent.

Firstly, if we power the CMOS from 15V, (actually +/− 7·5V) the 'on' resistance is at its lowest and varies least. The op-amps we use should not mind working from the same supplies. Secondly, by positioning the switches next to the virtual earth point, when 'on', the voltage on the transmission channel is never very far from zero, and the resulting swing in 'on' resistance is kept to a minimum. The 'on' resistance is very small compared to the normal range of values of input resistor, (300Ω as a very maximum) and the off resistance is typically IOM which is an open circuit for all practical purposes. In experiments carried out using a 4066, as hold and set switch, with a 1μ capacitor charged to 1V, the droop rate of the stored voltage was about 1mV per minute. Fig 9 shows an integrator with transmission gate set and hold switches, plus one for a simple range switch. The 'on' resistance of the gate limits the current which flows when the set switch is closed.

CHOOSING AN OP-AMP

The op-amp we use can be a variety of types, the most important criterion for high performance circuits being input bias current. Fig 10 shows a circuit which will not work (guaranteed – I know 'cos I was there, although I deny all responsibility for its design, honest officer) for a number of reasons. The symptoms were, that the amplifier could not be zeroed, that the output voltage jumped when the set button was released and then ramped quickly away, and that when the input was grounded the output voltage ramped quickly back down to a poor almost-zero. Not terribly good behaviour for an integrator.

A lot of these undesirable effects can be explained in terms of input bias currents. Looking at the specification of the chosen op-amp, (a 725) we saw that the input bias current was some 80nA max. Input bias current is defined as the average of the input currents flowing into the input of the op-amp. The input offset current is the difference between the two bias currents when the op-amp output is a zero volts; in this case only about 1nA. The bias currents for this device are very well matched, yes, all right, but are large by comparison with what we would like.

NO WONDER THE OP–AMP WON'T ZERO

Now if we work out the voltage across the invverting input resistor and the non inverting input resistor, 100k and 47k respectively, we get 8mV on the inverting input and a little less than 4mV on the non inverting input, which amounts to a voltage differential of more than 4mV; multiply this by the open loop gain (127dB) and there is no wonder the amplifier will not zero. In practice, as the output voltage swings, the bias currents change, and the equilibrium position is a few hundred millivolts from zero.

In practice, as the output voltage swings, the bias currents change, and the equilibrium position is a few hundred millivolts from zero; but this is still too much to null. All this illustrates the reason for keeping the impedances on the two inputs of an op-amp the same – it 'reduces offsets', and it is good practice on any op-amp circuit especially where high gains or precise zero dc levels are needed. We can get away with having unbalanced inputs if we are building a voltage reference or regulator circuit, which just has to sit at 10·00V for instance, but we cannot get away with it in any situation where a true zero out is needed for zero input.

The bias currents are also responsible for the initial 'jump' when the set switch is released. With the switch closed, the bias currents flow for preference in the

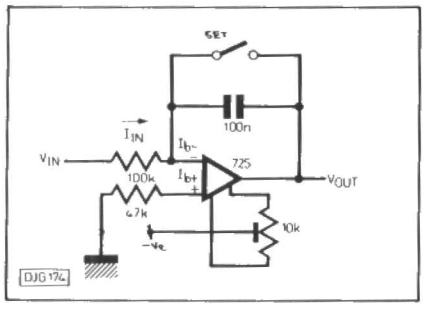


Fig.10. *The one that got away.*

switch, not through the input resistor. Immediately the switch is released, the voltage due to the 100k resistor is again imposed on the inverting input resulting in the jump described. Actually, making the nulling better makes the jump worse...

The ramping with no input current is caused by the bias currents charging the capacitor. At 80nA a 100nF capacitor will charge to 200mV in a quarter of a second; in practice it took a few seconds to do this. When the input resistor is returned to ground, the currents flow in it, plus some current from the capacitor which discharges it.

It may seem as though I am labouring this point about bias currents, but it really is the single most important factor in choosing an op-amp for integrator use, and causes more woe than you may imagine. Because they are usually so much smaller than the currents flowing in the feedback and input circuits, bias currents get ignored, with the results as explained.

SMALL BIAS

So choose an op-amp with the smallest input bias current generally available. Taking the 3140, which is an internally compensated 741 look alike, the specification says that it has an input bias current of 10pA max, four orders of magnitude better than the 725. When applied to the circuit above, the 'jump' comes down to less than a millivolt, and the trimmer can be adjusted to reduce the output voltage creep for zero input, to a few mV per minute.

Output creep is the term I use to signify that tendency of an integrator to integrate what is in theory a zero input, which is due to offsets and can be trimmed out. With the input open circuit, creep is replaced by droop, familiar to sample and hold circuit designers especially those who work all night. As explained above very low droop rates are obtained in practice.

An additional advantage of the 3140 is its 110kHz full power bandwidth, as opposed to a mere 10kHz for the 741. As far as filters are concerned, we have in the 3140 and its ilk the bandwidth to get high Q's in the upper audio bands, and the low input bias currents to use higher input resistances, for larger time constants and lower cut off frequencies. Thus we are able to push back the frontiers of audio filtering into the sub audio and the ultrasonic. As far as computation and wave form generation are concerned, the low level input biasing allows larger, more accurately defined time constants and more precise integration.

CURE THE DRIPPING TAP

The solution is to cure the dripping tap. If we must stop the integrator for periods of time, then we should fit a 'hold' switch rather than relying on it not to creep. Also we can practically eliminate the creep by nulling with the standard nulling potentiometer. If we want a sort-of-integrator for one reason or another then plank in a resistor, but let's not have any such corruption if we want to measure or compute.

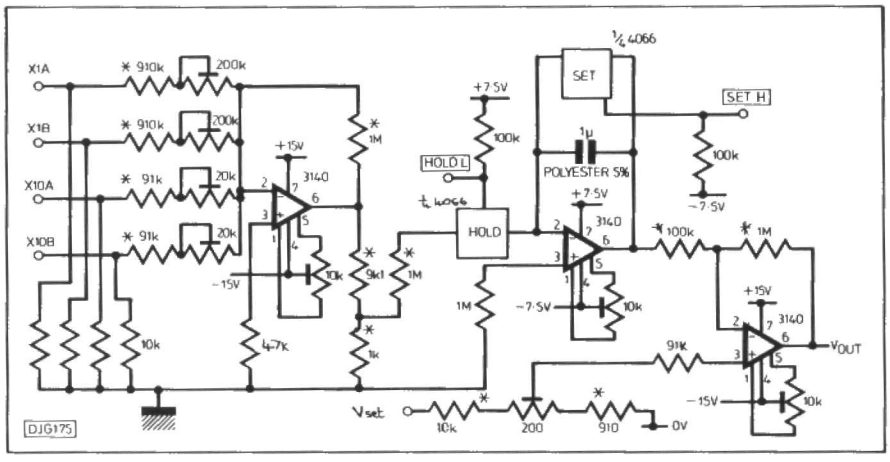


Fig.11. *High performance computation integrator (lights, camera, action).*

ROGUES GALLERY

Before going on to describe briefly a practical integrator circuit, a quick look in my collection of heinous practices reveals one or two that apply to the integrator. Apart from the aforementioned electrolytic capacitors and unbalanced input resistances, (Ugh!) there is the so called leaky integrator. Now there is really no excuse for this as there is always a better way to arrange matters. A resistor added across the capacitor, can you believe it, in an attempt to stop the output creep.

In a filter circuit there are feedback networks which work to keep the output stable in the absence of an input signal. With a wave form generating integrator the circuit is cycling continuously and any creep is expressed as an error in the frequency. But in the computation integrator, and more so in the measurement integrator, the input may be zero for periods of time and the integrator must not creep if we can possibly avoid it.

To turn back to the resistor-across-the-capacitor lark, if we liken our capacitor to a bucket and the input current to a running tap, then the leakage resistor is like cutting a tiny hole in the bottom of the bucket. This is all right if the tap is just dripping and we want the bucket to stay empty, but if we then run the tap, as the bucket fills up the water runs out of our little hole faster and faster until it keeps pace with the tap – i.e. our integrator is an integrator no longer. Worse yet, when we want to turn off the tap and hold our level steady to measure it, it is falling away before our very eyes!

Fig 11 shows a computer integrator circuit, built with easily available components. Some features of this circuit require explanation. The first and third integrator op-amps are powered from +/– 15V to get the +/– 10V range required as standard from an analog computer element. The second op-amp is powered from the CMOS supplies to prevent damage to the CMOS. An attenuator reduces the signal levels from the summer stage, and the final stage has a gain of –10 to push the levels back up to those needed. The overall operation is inverting.

PE

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NEXT MONTH OUR DESIGN FEATURE DEALS WITH ELEMENTS OF HI-FI. WE WILL HAVE AN INDEPTH LOOK AT THE USE OF COMPONENTS IN ALL AREAS OF HI-FI AND MUSIC RPOJECTS.

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EXPERIMENTAL ELECTRONICS

BY THE PROF

A shift of frequency

Change the speed of a tape recording without affecting the tone!

SHIFTING the frequencies in an audio signal may seem like an interesting but useless exercise, and it is a subject which has not received a great deal of attention in the past. However, there are practical applications for frequency shifting, or frequency division/multiplication (which is really a more accurate description of the process). The lack of attention the subject has received is probably due more to the difficulties involved than any real lack of practical applications.

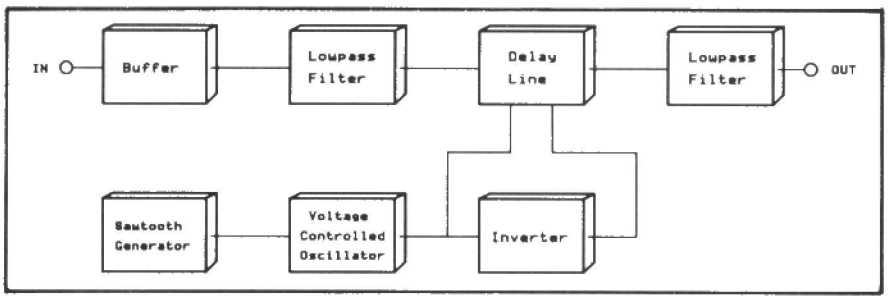


Fig.1. *Basic frequency shifter block diagram*

FIGURES OF SPEECH

An obvious application is in the field of electronic music, in 'harmonisers' and similar applications, where the processed signal is mixed with the straight-through signal to give richer and more interesting sounds. Another interesting application is in variable speed tape recorders. The general idea here is to have a tape recorder where the playback speed can be altered, but the pitch of the output is not subjected to the usual changes associated with wrong playback speed. The main purpose of this type of equipment is to enable dictation machines and similar gadgets to play back at two or three times normal speed without the pitch of the signal being doubled or trebled. This is not just a matter of getting the signal to sound right for the sake of it, and intelligibility is significantly enhanced by maintaining the original pitch, or at least something approximating to it. The point of speeding up the playback speed is simply that most people talk at something in the region of 100 to 120 words per minute, but can understand speech at speeds of 300 words per minute or even more. Speeded up speech can therefore rival reading in terms of what could be called verbal baud rate.

There are two general methods of frequency shifting signals, and these are the heterodyne and delay line systems. Taking the heterodyne method first, this is essentially the same as the system used to generate single sideband radio signals. The audio signal is mixed with the output of a carrier oscillator to produce sum and difference frequencies. A system of filtering or phasing is used to eliminate the difference in frequencies, leaving the sum frequencies which are effectively the input frequencies boosted by an amount which is equal to the carrier frequency.

Although it sounds simple in theory, it can be difficult to get good results from this system. By tuning in a single sideband radio transmission and varying the tuning either side of the correct setting, the upwards and downwards shifts in pitch can be heard, but only a modest amount of downwards shift can be achieved before the effective carrier frequency is placed within the frequency components of the input signal, resulting in it becoming scrambled. In fact in an extreme case the frequencies would become inverted (i.e. high frequencies would become bass frequencies, and low frequencies would be changed to high tones). This is a popular method of voice scrambling, and is a topic to which we might return in a later article.

The heterodyne system is limited in practical value by its inability to provide much downward shift, and by the fact that the harmonic relationship of the shifted frequencies is totally destroyed. This makes it unsuitable for many practical applications, including voice pitch correction in fast playback systems. The delay line system is much better in both respects, and it can provide large upwards or downwards shifts in frequency without altering the harmonic relationships of the constituent frequencies. In other words, rather than shifting frequencies up or down by a specified number of Hertz, this method multiplies or divides the frequencies by a specified factor. In the fast playback application, the doubling or trebling of the pitch can theoretically be perfectly counteracted by a delay line frequency shifter circuit.

The basic arrangement for this type of circuit is shown in the block diagram of Fig. 1. The top row of blocks represent a standard 'bucket brigade' CCD delay line having a buffer stage at the input, a lowpass filter, the delay line itself, and then another lowpass filter. The principles of CCD delay lines have been covered in Practical Electronics before, and will not be discussed in detail here. The general scheme of things is to sample the input voltage repeatedly, and to pass the sampled voltages along a series of charge storage capacitors before they finally emerge from the final capacitor at the output. This gives a stepped version of the input signal, but the final lowpass filter removes the steps and restores the original signal. Of course, it takes time for the samples to travel through the capacitor chain and find their way to the output, and the delay time is controlled by the number of delaying stages plus the speed at which the samples are passed along the chain. This second factor is controlled by a clock oscillator.

A voltage controlled oscillator (VCO) is used to provide the clock signal, and an inverter stage provides an antiphase signal so that the delay line is fed with

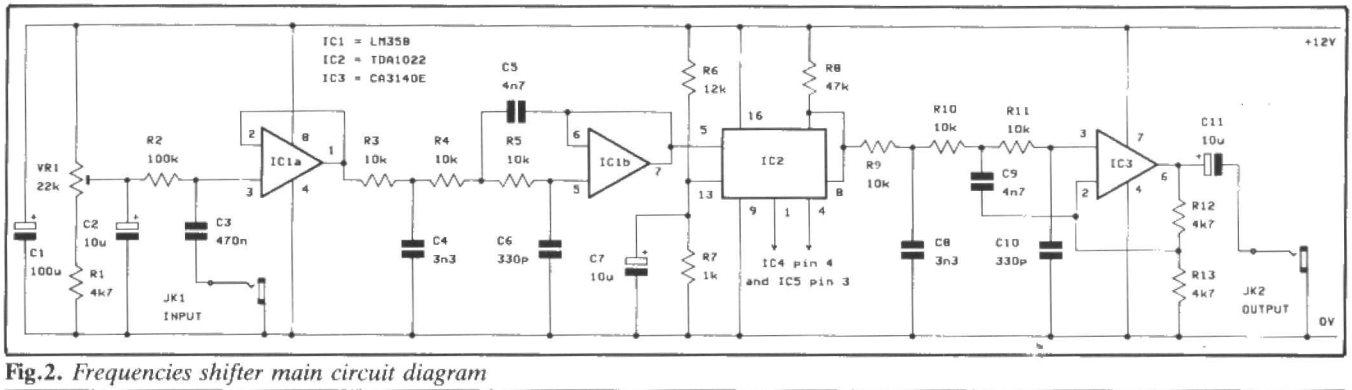


Fig.2. *Frequencies shifter main circuit diagram*

the required two phase clock signal. The voltage controlled oscillator is frequency modulated by a sawtooth generator. This setup is very much like a conventional vibrato effects unit, but the sawtooth generator would instead be a triangular type in a vibrato unit. Although one might expect the effect of modulating the clock frequency to be a steady fall in pitch as the frequency is swept downwards followed by a complementary increase in pitch as it is increased, this is not quite what happens. The pitch actually switches between a higher one than normal and a lower pitch, not a gradual swing from one to the other. This is analogous to the sudden apparent change in the pitch of a car's engine caused by the doppler shift as it speeds past.

An increase in pitch is produced by using a sawtooth waveform of the type where the voltage sweeps upwards, but in practice this does not seem to give very good results. The problem is basically just that when the signal returns to its initial (low) voltage the VCO is set to a low frequency, and it takes a long time for the samples within the chip to be clocked out. This effectively gives short bursts of boosted frequency signal with comparatively long periods of silence in between. This severely chopped up signal is of little practical value. Fortunately, most applications require frequency dividing and not multiplication, but it would probably be possible to improve results greatly from the frequency boosting system if necessary. Possibly a second

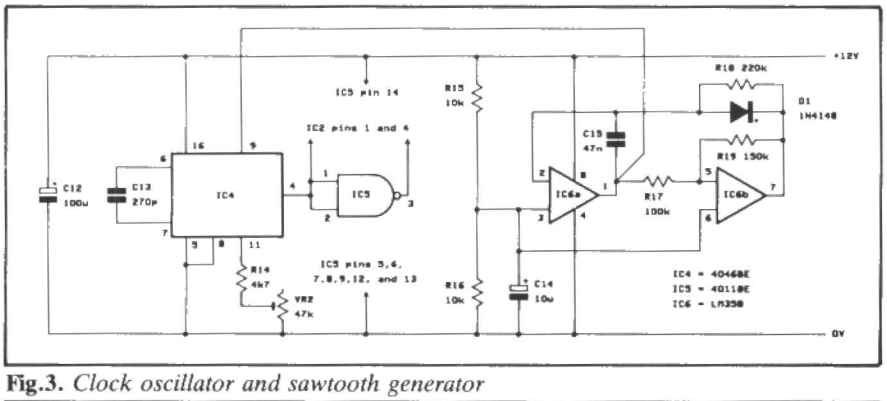


Fig.3. *Clock oscillator and sawtooth generator*

With a sawtooth waveform of the type having a downwards sloping ramp the effect is to give a reduction in the pitch of the output signal. However, when the sawtooth signal returns to its peak value the samples held in the delay line are suddenly clocked out at a much higher rate, giving a short burst of high frequency output. The number of output cycles is always equal to the number of input cycles, but what we are doing here is to have a long period of slightly reduced frequency followed by a short period of greatly boosted frequency. This gives an output signal which is predominantly at reduced frequency, but the short bursts of higher frequency are usually audible, although not as clear 'beeps' of sound. Just how well the glitches stand out, and the exact sound they produce, depends on the nature of the input signal.

delay line could be used to recycle the signal and provide a signal to fill in the gaps. Anyway, here we will only consider frequency reduction, which represents a somewhat less difficult technical problem.

BASIC CIRCUIT

Nothing terribly complex or expensive is required for a basic frequency shifter of the type outlined in Fig. 1, and a practical frequency shifter circuit is shown in Fig. 2 and Fig. 3.

Taking Fig. 2 first, this is a conventional bucket brigade delay line circuit having IC1a as the input buffer stage, and IC1b as an 18dB per octave lowpass filter with a cutoff frequency of about 10kHz. IC2 is the delay line itself, and the TDA1022 is a 512 stage type. IC3 is another 18dB per octave 10kHz lowpass filter, but it has been modified slightly in order to give about 6dB of voltage gain to compensate for losses through IC2.

Turning now to Fig. 3, IC4 is the clock oscillator, and this is the voltage controlled oscillator section of a CMOS 4046BE phase locked loop. The other sections of this device are ignored. In the past I have used one of the phase comparators in the 4046BE as an inverter to generate the second clock phase, but some recent 4046BEs seem to provide a non-inverted signal from the phase comparator if this is tried. IC5 (a CMOS two-input NAND gate wired as an inverter) is therefore used to provide the antiphase clock signal.

IC6 functions as the sawtooth generator, and this operates in what is almost a conventional triangular/squarewave oscillator circuit. However, the addition of D1 results in the positive going part of the waveform being greatly shortened due to D1 effectively short circuiting timing resistor R18 on this part of each output cycle, and the output

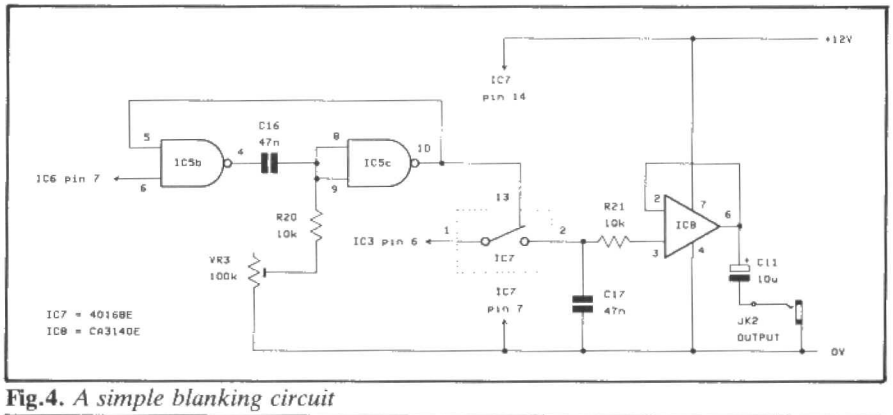


Fig.4. *A simple blanking circuit*

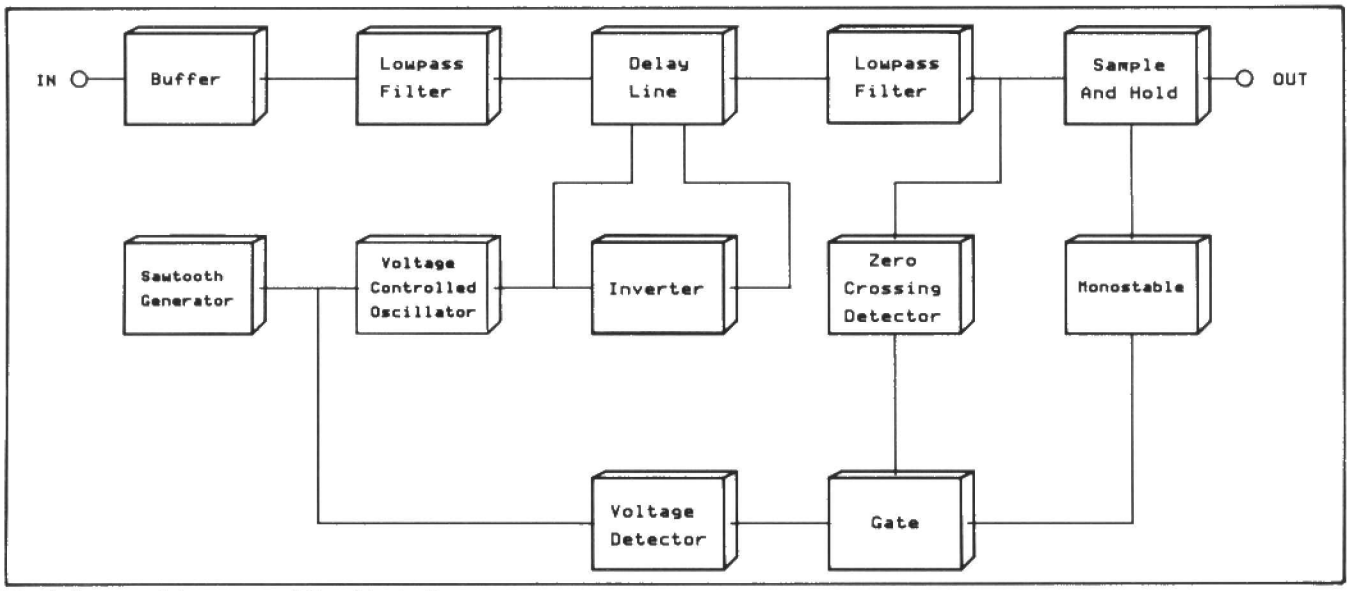


Fig.5. *Improved frequency shifter block diagram*

waveform is modified to the required downwards sloping sawtooth type. If you would like to try the circuit as a frequency booster, reversing the polarity of D1 will change the output signal to a positive ramp. It might be necessary to trim one or two circuit values in order to give a suitable output voltage swing for IC4 though.

There are two preset resistors in the circuit, and VR1 is simply adjusted for symetrical clipping, and the circuit can handle signals of up to several volts peak to peak. VR2 controls the output frequency range of IC6, and for maximum effectiveness it should be set for the longest maximum delay comensurate with good audio quality. The clock frequency needs to be at least double the maximum input frequency for acceptable results, giving a minimum clock frequency of about 20kHz. This is about the minimum acceptable anyway if audible breakthrough of the clock signal at the output is to be avoided.

RESULTS

The circuit certainly produces a downwards shift in frequency, but it also gives a lot of strong glitches on the output which ruin the audio quality. To some extent the unwanted output signals are due to breakthrough of the modulation signal at the output. This is due to changes in clock frequency producing variations in the quiescent output voltage of the delay line, and this is something that is common to all the CCD delay line chips that I have encountered. The problem can be greatly reduced, although not eliminated, by connecting a 2M2 linear preset between pin 3 of IC3 and pin 1 of IC6. The breakthrough at the output is out of phase with the sawtooth output from IC6, and the preset can be adjusted to optimise cancelling of the breakthrough.

One obvious refinement to the basic scheme of things would be to blank the signal during the glitches, and Fig. 4 shows the circuit of a suitable blanker. This is based on a sample and hold circuit which has CMOS analogue switch IC7 to cut off the signal, and C17 to maintain the signal level during the blanking period. IC8 merely acts as an ultra-high input impedance buffer stage so that the charge on C17 is not significantly altered during the blanking period. This part of the circuit is added in series with the output of the original circuit, with C11 and JK2 being transplanted from the original circuit to this one.

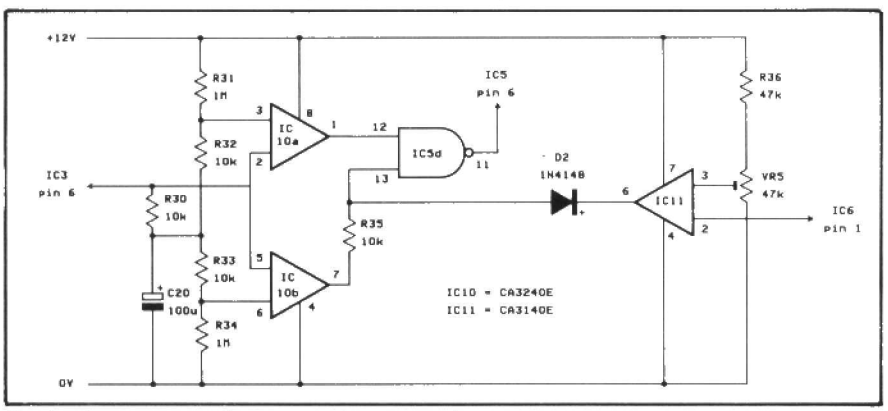


Fig.6. *Zero crossing detector and gate circuit*

The blanking pulse is generated by two of the previously unused gates of IC5, and these are connected in a standard CMOS monostable configuration. This is triggered from the pulse output of IC6, which generates a brief negative going pulse at the end of each cycle. VR3 is adjusted to give an output pulse that is just long enough to blank out the burst of high frequency output signal.

In use this circuit is not particularly effective, and the problem is one of switching glitches as the signal is switched on and off. This can produce worse interference on the signal than the glitches from the delay line. This problem can be overcome to a large extent by using the modified arrangement shown in the block diagram of Fig. 5.

This is much the same as the original, but it has the addition of the blanking circuit (the 'sample and hold' and 'monostable' blocks), plus a more complex means of triggering the monostable. The general idea is to blank the signal as it passes through the zero voltage point, and this is achieved by triggering the monostable from a zero crossing detector which provides a suitable output pulse each time the output signal passes through the zero volts point. This arrangement is unworkable since it would trigger the blanking circuit each time the signal went through zero, whereas we only require the blanking action when the signal goes through zero volts and the signal from the sawtooth generator is at or near to its minimum level. A voltage detector is therefore used to detect when the sawtooth signal has almost reached the end of a cycle, and via a gate circuit this enables the zero crossing detector to trigger the monostable.

The circuit diagram of the zero crossing detector and gate circuit appears in Fig. 6. The zero crossing detector is actually a window

discriminator based on IC10, and the outputs of both devices go high when the input signal is at or very close to the zero level. An accurate reference voltage for this circuit is obtained by using R30 and C20 to produce a smoothed version of the output from IC3. IC5d is the remaining NAND gate of IC5, and it produces a negative trigger pulse for the monostable when both its inputs are taken high. However, voltage detector IC11 clamps one input of IC5d low until almost the end of each sawtooth cycle. IC11's output then goes high, leaving the relevant input of IC5d to go to either logic state, as dictated by IC10b. VR5 is adjusted to give a suitable enable point on the sawtooth cycle, and as with most of the other adjustments associated with this system, it is a matter of setting this preset for what subjectively gives the best results.

Results are substantially improved by the zero crossing circuitry, with the glitches rendered far less severe, although still quite obvious on most signal sources. Another advantage is that a combination of suitable blanking pulse duration and the cancelling circuit mentioned earlier seems to eliminate totally any breakthrough of the sawtooth signal at the output, giving a silent background under quiescent conditions. On setting an old cassette mechanism to give speeded up playback of a voice recording the unit certainly brings the signal back down to a more natural pitch, but it would be an exaggeration to say that it gives perfect results.

An interesting way of using the system is to employ the ring modulator circuit of Fig. 7 to mix the shifted and unshifted signals. Ring modulation gives metallic gong and bell type sounds, but with the conventional method of having the input mixed with the output of a fixed frequency oscillator the sound obtained depends very much on the input frequency. Some notes provide excellent sounds, while others sound far from harmonious. With this system the musical interval between the two mixed signals is constant, and so is the effect obtained. VR4 can be adjusted to balance out the input signals so as to leave only the sum and difference frequencies, but in practice it would normally be set to let through the input signal quite strongly and in effect to mix it with the sum and difference frequencies.

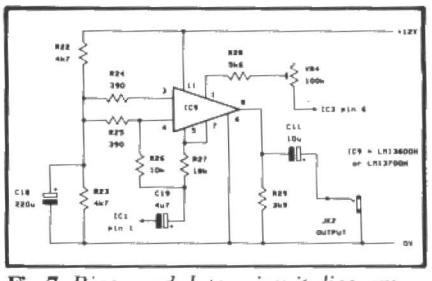


Fig.7. *Ring modulator circuit diagram*

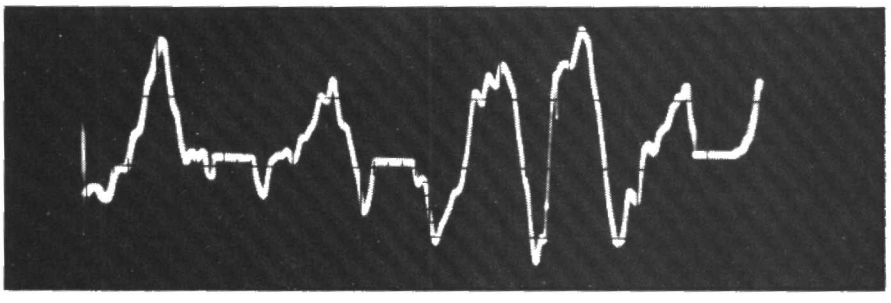


Photo.1. *Blanked periods seen in short speech signal*

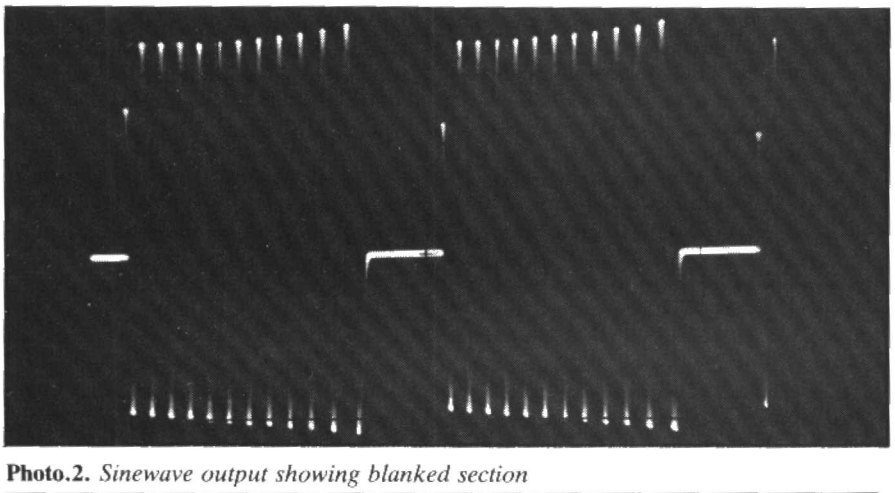


Photo.2. *Sinewave output showing blanked section*

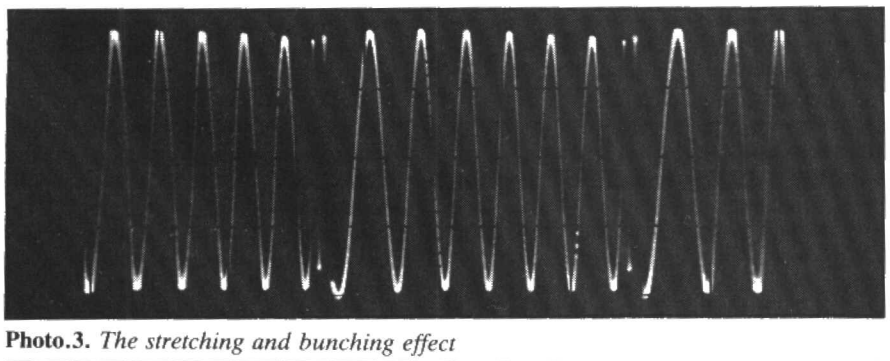


Photo.3. *The stretching and bunching effect*

IMPROVEMENTS

The system as described here certainly works quite well, but definitely leaves room for improvement. The degree of shift can be altered by varying the operating frequency of the sawtooth generator, but this frequency can not be boosted very much without producing side effects which make the system unworkable. To obtain large shifts a longer delay line would be needed, and the TDA1097 1536 stage device (as used in some fairly recent PE projects) is the obvious candidate. Although it might seem a good idea to use a very long delay line with a low sawtooth frequency to give infrequent glitches, this does not work well, as it tends to chop the signal so that quite long chunks are cut out and, if taken to extreme, complete syllables or even whole words would be eliminated.

To some extent the remaining switching glitches on the output can be counteracted by using lowpass filtering. However, the best way of tackling them would be to improve the zero crossing circuits. At present they ensure that the cutoff occurs as the signal goes through zero, but it is switched on again as soon as the monostable pulse ceases, regardless of the signal voltage at that instant. There should be a worthwhile improvement in the output signal quality if the circuit was arranged so that the monostable pulse was effectively elongated until the signal passed through zero volts again. With this refinement the system would probably be developed as far as would be worthwhile. Further improvements would probably give little real advantage and could be implemented more easily and effectively in a digital system – which is another story. PE

NEXT MONTH
SCRAMBLING CIRCUITS

PE PROMENADER

PART ONE BY MIKE DELANEY

A stand-alone programmer without a computer!

We have had lots of letters in recent years expressing concern that hobbyist electronic magazines, PE included, carry too many computer projects. With this in mind we bring you an EPROM controlled disco sequencer/programmable display which doesn't need a computer to programm it!

"ANYONE who has had to sit through a typical disco-light display such as I had to a while back would gladly suffer a power cut!" said a friend of mine. This led to a discussion about the complexity of a 'good' system, and set me off to thinking whether it would be feasible to load a program into a memory device of some sort, tape, disc or ROM, for recall later.

The friend that made the remark is also a disco operator, but is not particularly switched on when it comes to programming. Thus whatever system was to be used must be simple to proramme, preferably without even mentioning the word.

I dare say that many constructors are put off a project once they see that PROMs are involved, since this almost always requires either hours of laborious HEX-DUMPING, or having to send away for ready programmed PROMs.

Due to the complexity and expense of discs, and the unreliability of tape, it appeared that PROM was the only answer. EPROM of the 32K calibre are very reasonably priced now, and it seemed a good idea to pursue this approach.

32k of PROM is made up of 4096 bytes of 8 bits, but how best to use it? This was answered quite by accident, in fact while I was thinking of the possibility of using a dot matrix printer drive chip. This was when the possibility of a 5 by 7 matrix started to become a reality.

Having a system which would allow the use of PROMs as storage space would, if tackled in the right way, enable the disco operator to turn up at a gig with a pocket full of programs, so the audience should never get bored.

Having got this far the only problem to overcome was that of the programming. It had to be simplified to the stage of 'press and see the result', by having a built in display of l.e.d.s. It was with all these considerations in mind that the final design was developed. And now, of course, I have to ask myself why I did not use a processor in the first place. There are a lot of chips in the programmer, but they are in the main fairly easy to obtain. The machine can be seen to be working, more than can be said for a processor-based unit, where it's all in the firmware. And, of course, it would still be necessary to obtain the system firmware in order for the system to run . . .

So what we are left with is a fairly complex board, double-sided and some pretty fine track, but a tried and tested system which has been giving excellent service for some time, and can be operated by a person who has no experience of programming.

THE FINAL DESIGN

Before getting down to the nitty-gritty of explaining how the Promenader works it might be as well to have a summary of all the facilities available.

Following power up the RAM will contain any amount of rubbish in all the address locations. In order to make it possible to locate the end of the recorded data they must all be set high. This is achieved by selecting ROM PLAY, with S3, leaving the EPROM socket empty, and transferring data from ROM TO RAM, with S5. By omitting the PROM the data lines are pulled high by resistors, as is standard tri-state practice. This will leave the RAM clear for programming. The state of an apparently clean EPROM may be verified by S4, ROM CHECK, when in Rom Play mode. If any bit of the 2046 should be set low the address clock will stop, and the display will show the location of the error. This saves a lot of time when loading a PROM, and was added to the unit after an apparently erased PROM created an unexpected display!

In order to add to an existing program, where space remains on the PROM, it is necessary to transfer the program already stored, to the RAM, and this is done by selecting ROM PLAYand ROM TO RAM together. Since ALL the data are transferred from the PROM, it is convenient to leave the transfer running after the last of the recorded data, so that the unprogrammed 1's are also transferred to the RAM ensuring that the rest of the RAM space is clear.

The display is made up of 40 LEDs, 35 of which are the model for the finished display, and the other seven, located to the left of the matrix are an indicator as to which ROW is being pogrammed. The ROW select switch, S8 is successively pressed to clock down the rows, and cycles round to the beginning for corrections etc.

The individual lamps are set HIGH or LOW (ie. the LED is LIT or OUT) by pressing one of five switches, S13 to 17, each of which corresponds to one COLUMN of the five. These TOGGLE switches may either set high or low, depending upon the position of the +/− switch, S10. The plus sign indicates a high, and the led would be lit when the toggle is pressed and the polarity switch S10 is not pressed. Pressing down S10 when a toggle switch is selected will set that particular bit LOW, and the LED will be OFF.

Switch S7, NEW PROG must be ON before a programme can be recorded. This switch is used to access the data to the RAM only, and does not change the data on PROM.

When making up a program it was found that most of the time the lamps were made to 'BUILD UP' from a simple start with perhaps only one lamp on at the start of a sequence, to all on at the end. The prototype automatically extinguished all the lamps after each group of 7 had been dumped to RAM, but this was changed on the final design to leave them unchanged. This was found to reduce programming time and errors many times over.

Switch S12 RESET DISPLAY will, however, switch all the LEDs off if required.

RESET ADDRESS switch, S11, is useful when running back over a program. Depressing it sets the address bus to 000, and allows the memory to be read from the beginning.

'END' is not a self-destruct instruction, but another time-saver. Depressing it when in either RAM or ROM PLAY will automatically halt the system clock at the end of the recorded data. This makes adding or correcting very much easier, since the electron is faster than the finger!

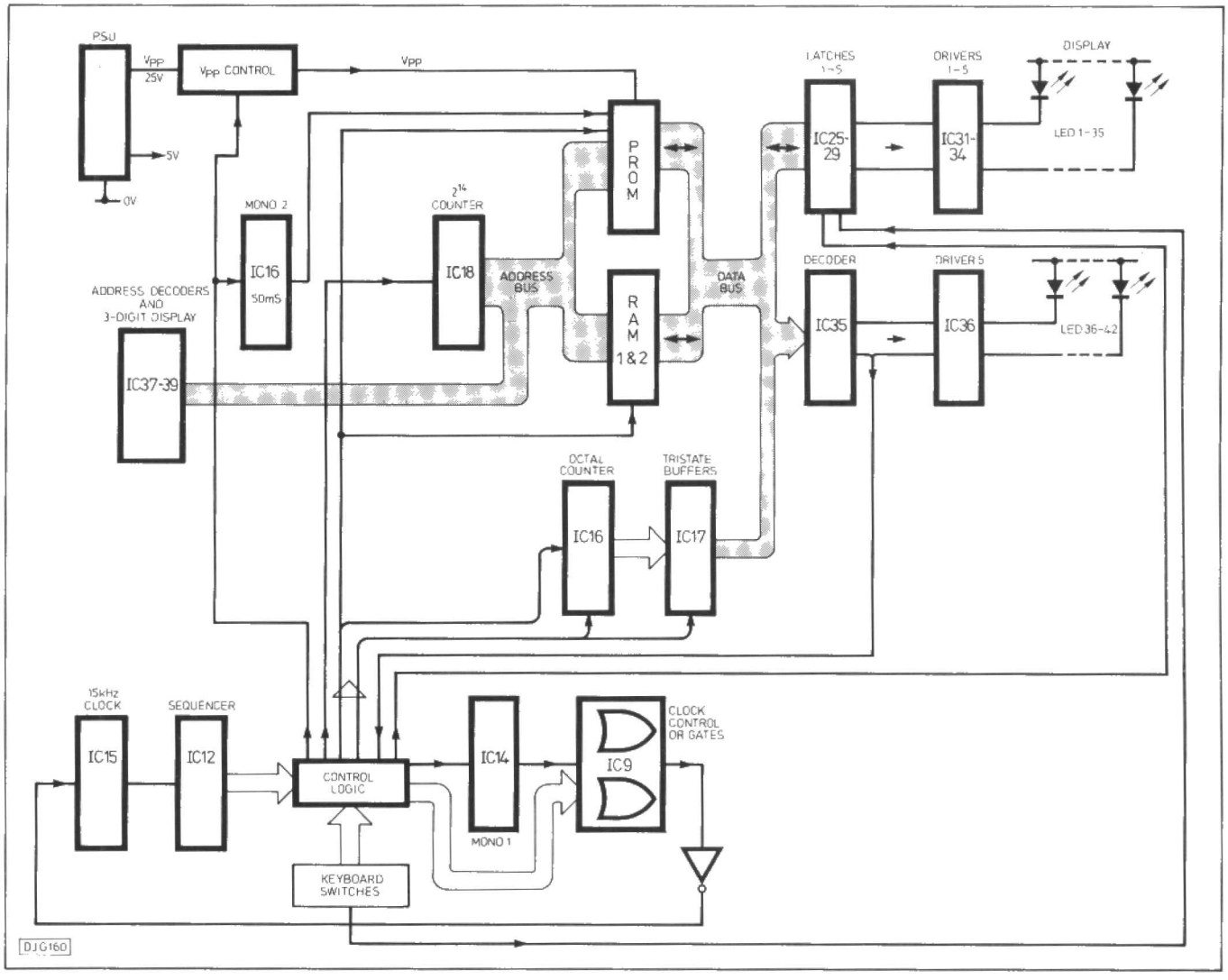


Fig.1a. *Programmer block diagram.*

The programming of the PROM is achieved by selecting RAM PLAY and then ROM PROG. An indicator is used to confirm that the programming voltage, VPP, is present at the ROM.

The unit will, and in fact has functioned as a crude PROM copier. I use the word 'crude', since there is no check that the data has been transferred correctly, so be wary of using it for any particularly demanding copying. I was going to incorporate a check of some sort, thus increasing the flexibility of the unit until I realised the complexity of a reasonably foolproof check. This type of unit is very definitely best left to a processor circuit.

The pause time between each seven bytes is variable, from a very slow rate – so that all the bits can be checked, and the clock halted with the NEW switch if required – to a high-speed get-there-quickly. This latter speed is most useful when going back over a new program during its creation. I had not realised how fast a flash of inspired brilliance could become the most monotonous and repetitious bore until I made up a full 2046 bytes in one sitting. That was all that was needed to bring in the high speed mod!

This completes the overview of the system, and I am the first to comment that it really SHOULD have been done using a processor. However, my friend (the guy hoping for the power cut) got his super disco display in about a quarter of the time it would have taken to develop such a system. Certainly there are a lot of chips, but the Promenader does afford a lot of facilities, and at quite a reasonable price.

DATA ORGANISATION

Having decided to use a 7 x 5 matrix of lamps it remained to sort out how best to organise the way in which the programs could be easily stored, recalled and decoded.

One byte of eight bits lends itself neatly to coding as five data bits, and the remaining three as address bits, and this approach is the one chosen. In this design the highest three are used as the address bits. Fig. ? shows a typical arrangement of data as it would appear if it were listed as 1's and 0's, and is the sort of pattern which might easily be used.

The most significant three bits are a repeated BCD count from one to seven. The other five bits are the recorded data which drive the lamps in the display. A '1' in these five represents a 'Lamp On' on the output. It is worth noting that when a program has been stored a BCD 7 (111) in the MS three is ALWAYS followed by the BCD 1 (001).

However, this will not be so when the end of the recorded data is reached. Since the EPROM is erased to leave all bits HIGH (1) the end of any recording will be followed by another BCD 7. It is this sequence of data which is used to detect the end of the recording, or if there are no EPROMs present, since the data lines are pulled HIGH, by resistors.

Using this method of storage has the advantage of being comparatively easy to decode later. No special synchronising or timing pulses or clocks are required. Since the address is also part of the stored information, all that is needed is a BCD counter to ensure that the correct data is presented at the right time for further processing.

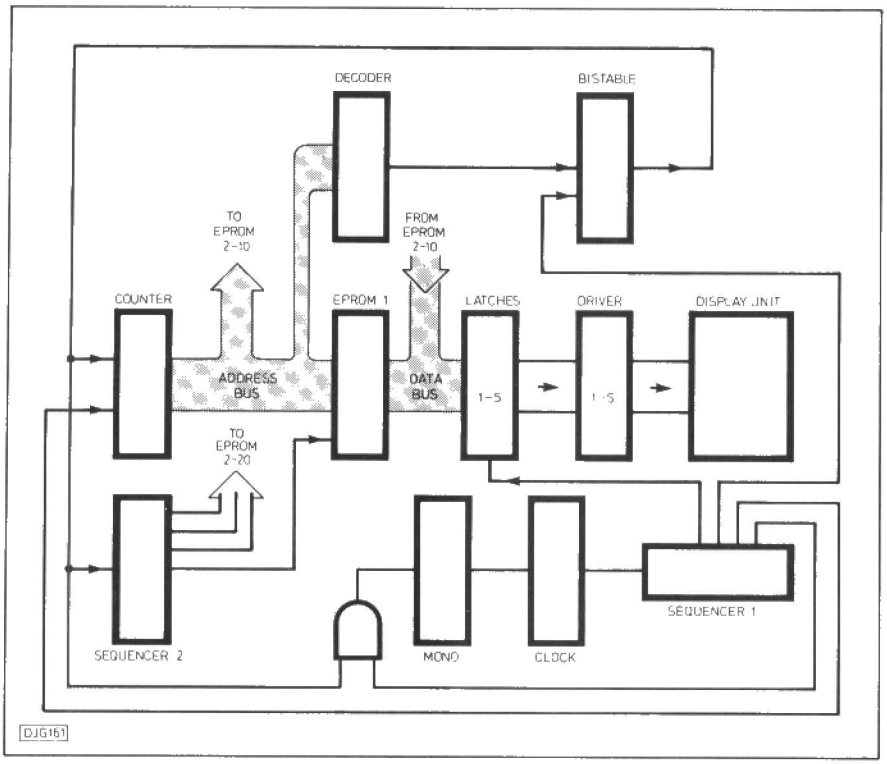


Fig.1b. *Display block diagram.*

Naturally enough, there is a trade-off. In this case the trade is in the form of more involved storage and presentation of the data to the outside world. This was considered a fair trade following early tests on synchronous systems. One glich on the supply, and the whole program would change. Sounds OK, until the program consists of some lettering! Then you might be insulting a person in a foreign language, and not even know it! During normal use it was found that recording was a fairly demanding pastime. One lapse of concentration and at best you would have a quick correction of the lamps to do. At worst the EPROM would be residing in the eraser (AGAIN!!!).

To overcome this the data are first stored in RAM, from which it may be checked, overwritten if required, and finally stored on PROM. From this, it was decided to add the facility of data transfer from PROM to RAM as well.

Now we were able to record some of the program, pop down the road for a swift half and return later to correct all the mistakes we'd made before we went out!

This did open up the possibility of adding to an existing program. Fig. (a) to (e) show clearly how the data bits appear during a sequence of five sets of seven bytes. It would be a very difficult task indeed to produce a HEX-dump of such a sequence, and then follow it during a programming period.

BLOCK DIAGRAM

Fig. 1 shows the block diagram for the programmer unit. The system clock is a controlled astable, oscillating at about 15kHz. This is started and stopped by the control logic, by two three INPUT OR gates.

The timing of the control logic, and hence the complete system, is carried out by the sequencer.

Inputs to the logic is from either the keyboard, or from certain of the data bits in the recorded program in memory. The keyboard is made up of 17 switches in all, some of which are latching, but most are press to make. The keys are non-encoded, that is to say, all the decoding is done within the logic, and is entirely static.

Outputs from the control logic go to the memory and output stages of the circuit.

The address bus is driven by a buffered CMOS divider counter chip. It is not necessary for this bus to be tri-state, which helps in reducing the complexity of this stage. The data bus must be bi-directional of course, enabling the exchange of data between the memory chips and also the latches which follow.

During the recording stage part of the data encoding is made up of a three bit BCD code which is a count from the control logic into an octal/decimal counter. The output from this is tri-stated onto the data bus via a tri-state buffer. All the other chips on the bus have their own enable lines for bussing purposes. Data from the bus is latched through to output drivers, current limited by resistor networks, and displayed on 42 LEDs.

Also displayed is the HEX address which is present on the address bus. This is done by three special purpose decoder chips, and is used to drive three .5" seven segment LED displays. Having the address displayed in this way is vital when adding or correcting data onto a memory chip.

Programming the 2532 EPROM is straightforward enough, provided you observe a few basic rules. The programming voltage must lie between 24 and 26 volts, and the programming pulse applied to the memory must not exceed 55mS. Mono 2 is the programming timer, and must be set up at test, and prior to attempting to blow any PROMs. Again, the control logic is used to access this mono, and also the 25v programming voltage from the power supply.

Another requirement of the 2532 is that the programming voltage (VPP) is not applied to the memory unless the 5 volts is present at the supply pin first. This is taken into account by the VPP Control input to the power supply.

There is always a problem when designing a circuit such as this, requiring, as it does, two completely different voltages, +5v and +25v. Transformers with these windings are difficult to find. In the Promenader this particular problem has been solved by the use of a switch-mode power supply, which converts the output from the transformer to the required levels.

The RAM is made up of two 2k chips, only because 4k RAM is just about unobtainable. This is no great problem, since each half of RAM can be accessed in turn by using the enable lines. Provided both RAM are not enabled at the same time no data corruption should occur.

THE OSCILLOSCOPE

Figs. 2 and 3 show the complete circuit for the Promenader Programmer Unit. Oscillographs, A to K appear in Fig. 4. and these should be studied while reading the circuit description.

In order to make this description easier to follow I will explain the operations involved in firstly recording, then playback. Lastly the PROM programming will be described.

Starting with an apparently cleared EPROM in IC22, the first thing to do is to check that it really is fully erased.

Closing S3 and S4 will select ROM PLAY and ROM CHECK respectively. S3 takes IC2a/1 high and IC2b/6 low. Provided both S1 and S2 are open, 2a/3 will go high, taking 1d/11 low (TP6), and enabling the output from the PROM via the OE pin, 20. Pin 10 of IC6c will also go high, partly enabling the outputs of ICs 10b and 8c, though at this time 10b/6 will remain low and 8c/10 high.

ROM CHECK, switch S4 takes 3a/2 and 1c/9 high, and 1c10 immediately goes low, disabling monostable IC14, a 555 timer.

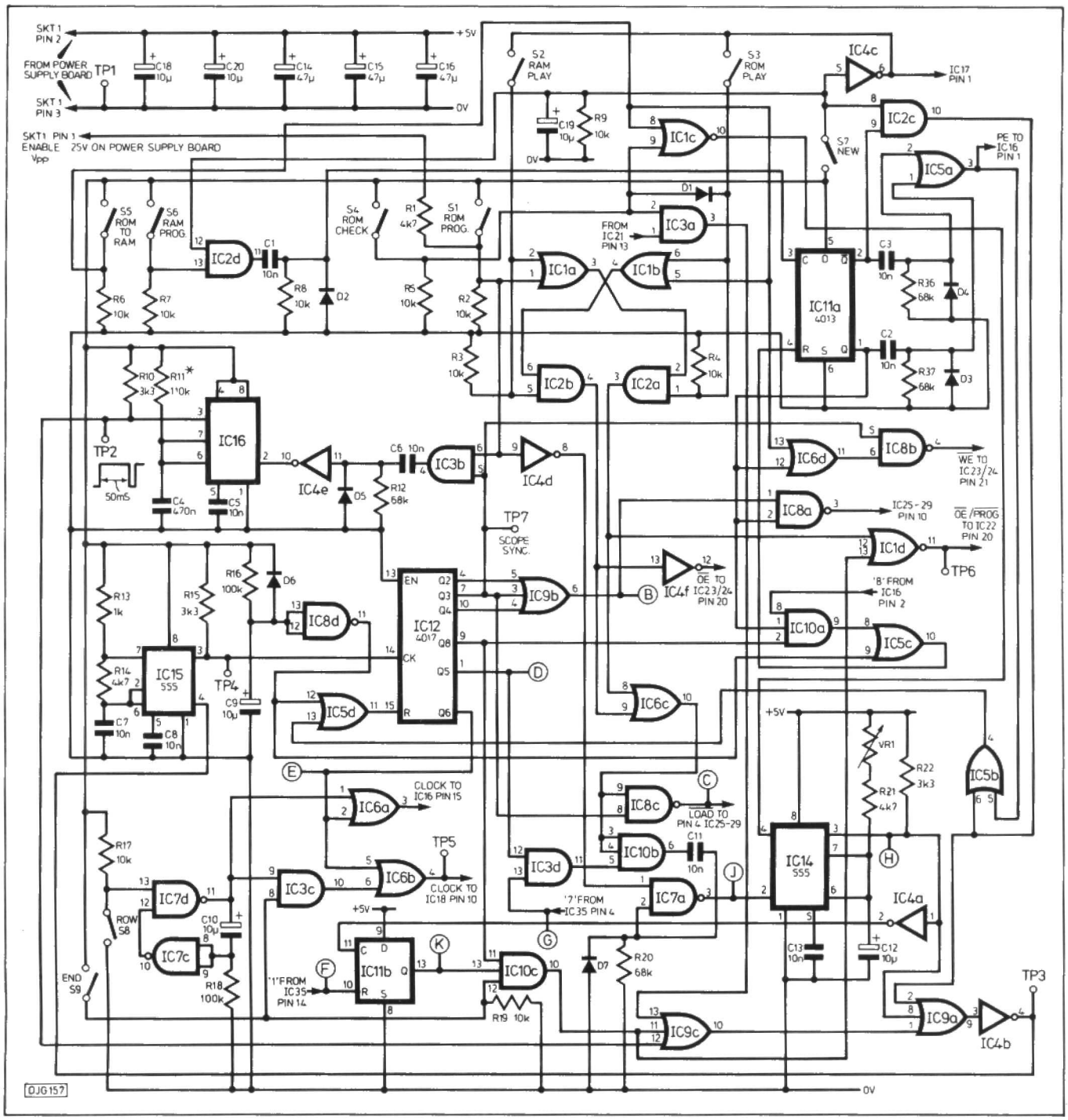


Fig.2. *Programmer circuit diagram.*

Pin 3 of IC3a will remain low provided pin 1 is also low. IC21 is a 4068, 8-input NAND gate, whose inputs are connected to the data bus, and its output will be low provided the DATA lines are ALL HIGH, ie. the PROM is clean. Thus 3a/3 will be low until an error is detected.

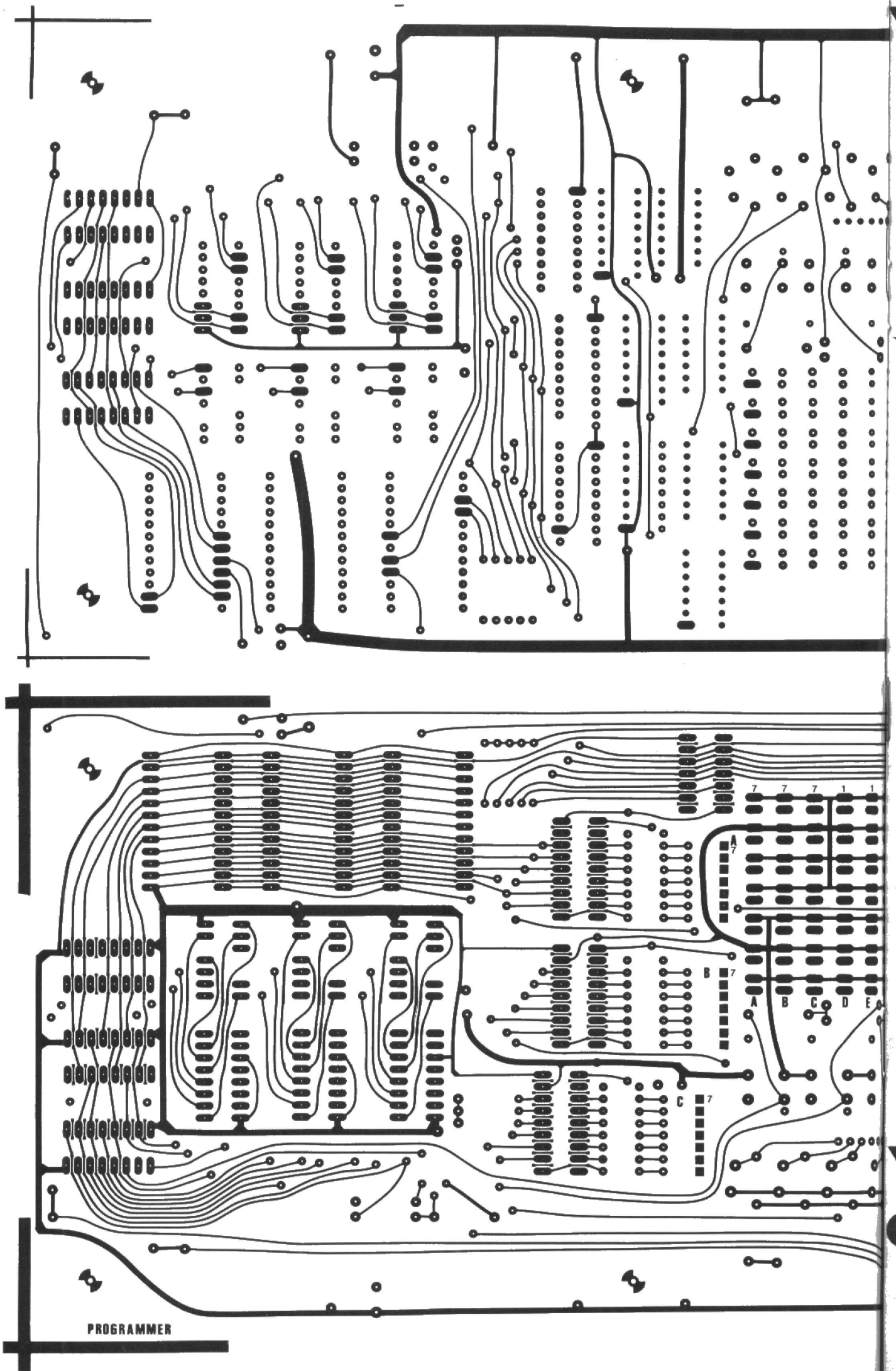
OR GATE 9c output is low until an error is detected, and this low is inverted by 4b, and appears as a high level at TP4, enabling the main system clock, IC15 via its control pin. Yes – yet another 555 – they get everywhere!

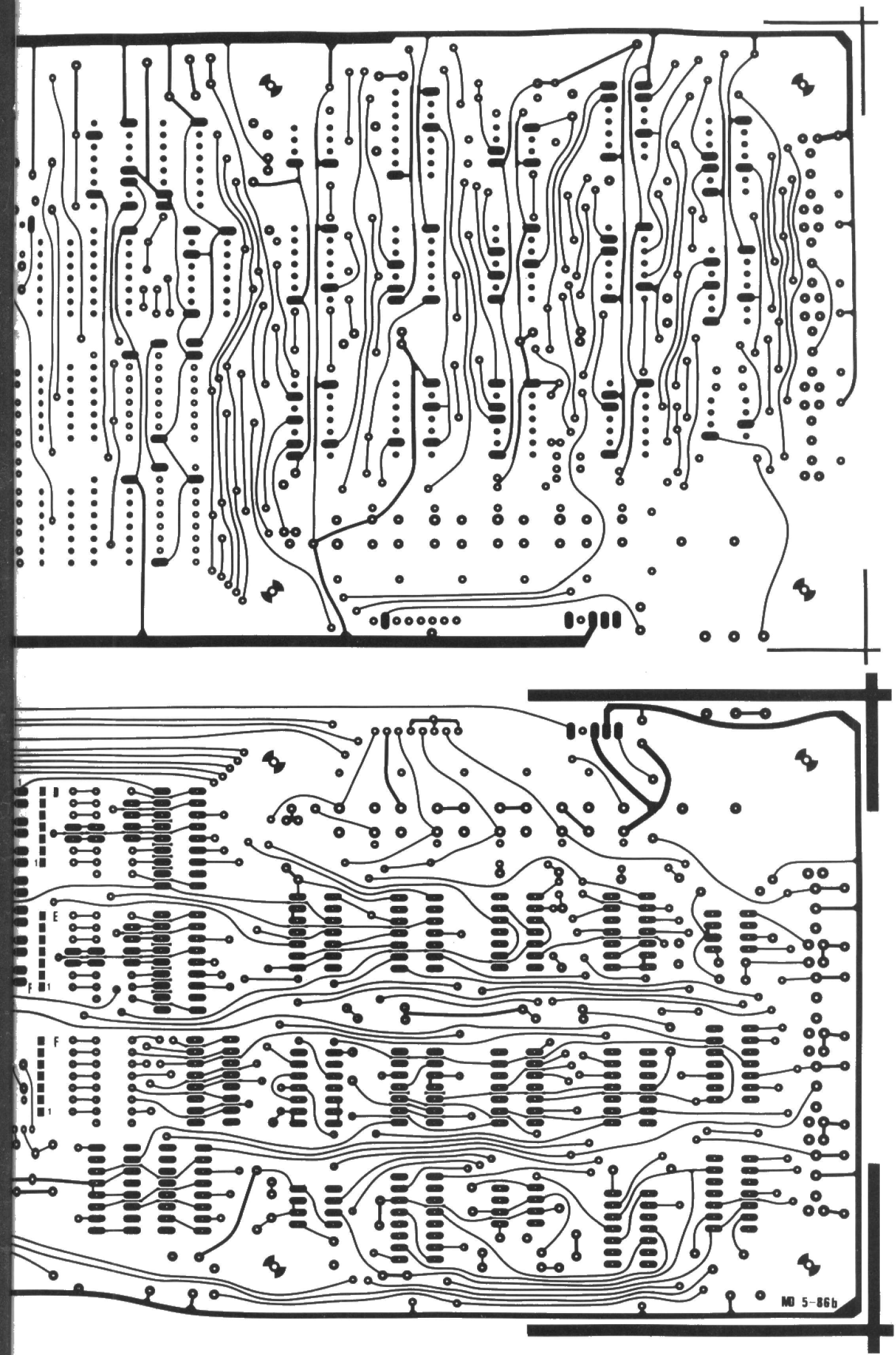
The system clock is therefore allowed to free-run at about 15kHz, which appears on TP4 and the clock input of the 4017 sequencer. The sequencer starts to cycle through, each of its outputs going high in turn. Q1 is not used, and in fact is to allow the system settling time, as are Q7 and Q9.

Tracing the outputs of the sequencer will reveal that only one of the outputs is used in CHECK mode, that is Q6, pin 5. All the other outputs are blocked by the logic gates.

Q6 is taken to 6b/5, and appears at TP5, and the input pin 10 of the address counter, IC18, a 4040. Thus the address coding changes at 15kHz/10, about 1.5 kHz. So it takes around 3 seconds to access all the address locations and complete a check. When an error is detected pin 13 of IC21 goes high, taking 3a/3 high also. 9c/10 and 9a/9 go high in turn, and the output of inverter 4b/4 goes low. This stops the system clock at the error address.

The 4040 is allowed to continue past the overflow stage, so that the check continues to run for as long as S4 is held down. Diode D1 bypasses S3 to ensure that the output data being checked is what is contained in PROM, and not RAM. It would be possible without D1 to mistakenly check the RAM if RAM PLAY switch were closed. The two NOR


7 7 7 1 1
A
7
B
7
C
7
A B C D E
PROGRAMMER


E
1
F
1
F
1
MD 5-86b

gates, 1a and 1b, disable the outputs of 2a and 2b, and ensure that only one switch may be on at a time. Should both S2 and S3 be on together, this would lead to data bus contention, since RAM and ROM would output at the same time. While the ROM CHECK is being carried out the address display will be cycling through, and the bottom line of LEDs will be lit on the display panel (since the data will be 11111111, corresponding to BCD address 7, all lamps ON).

Having satisfied yourself that the ROM is empty, and before starting to store a new program in RAM it is necessary to set all the data bits high in both RAM chips as well. This is done by transferring the data, all 1's, from PROM to RAM, with S5.

S3 is closed, to enable the data from PROM onto the bus, and S5 is closed.

Again, IC1b disables the RAM PLAY and IC14, but puts a high on 8b/5. The system clock starts and when Q3, pin 7 of the sequencer goes high, pin 4 of IC8b goes low. This is the WRITE ENABLE line in to the RAM, on pin 21. The data present on the bus is thus stored at the address selected. The sequencer then steps on, clocking the 4040 with Q6, and advancing the address count as it does. So each location is loaded with all 1's, and the RAM is clear to start programming.

THE LABORIOUS BIT!

The next stage is the laborious bit! If you wish to lose a friend ask him to program a couple of PROMs for you!

Closing S7, NEW, disables both playback switches, S2 and S3, via the inverter, 4c. The Q̄ output of 11a, pin 2 is set high on power up, by the reset circuit, 8d and 5c pin 10. IC2c/10 goes high, halting the system clock via 9a/2, and holds the sequencer in reset, with a high on pin 15, from gates 5b and 5d. So the system is completely stopped.

Data may now be entered on the latches with the TOGGLE switches. The latches, IC25–29, are each connected to one of the five lamp data lines through

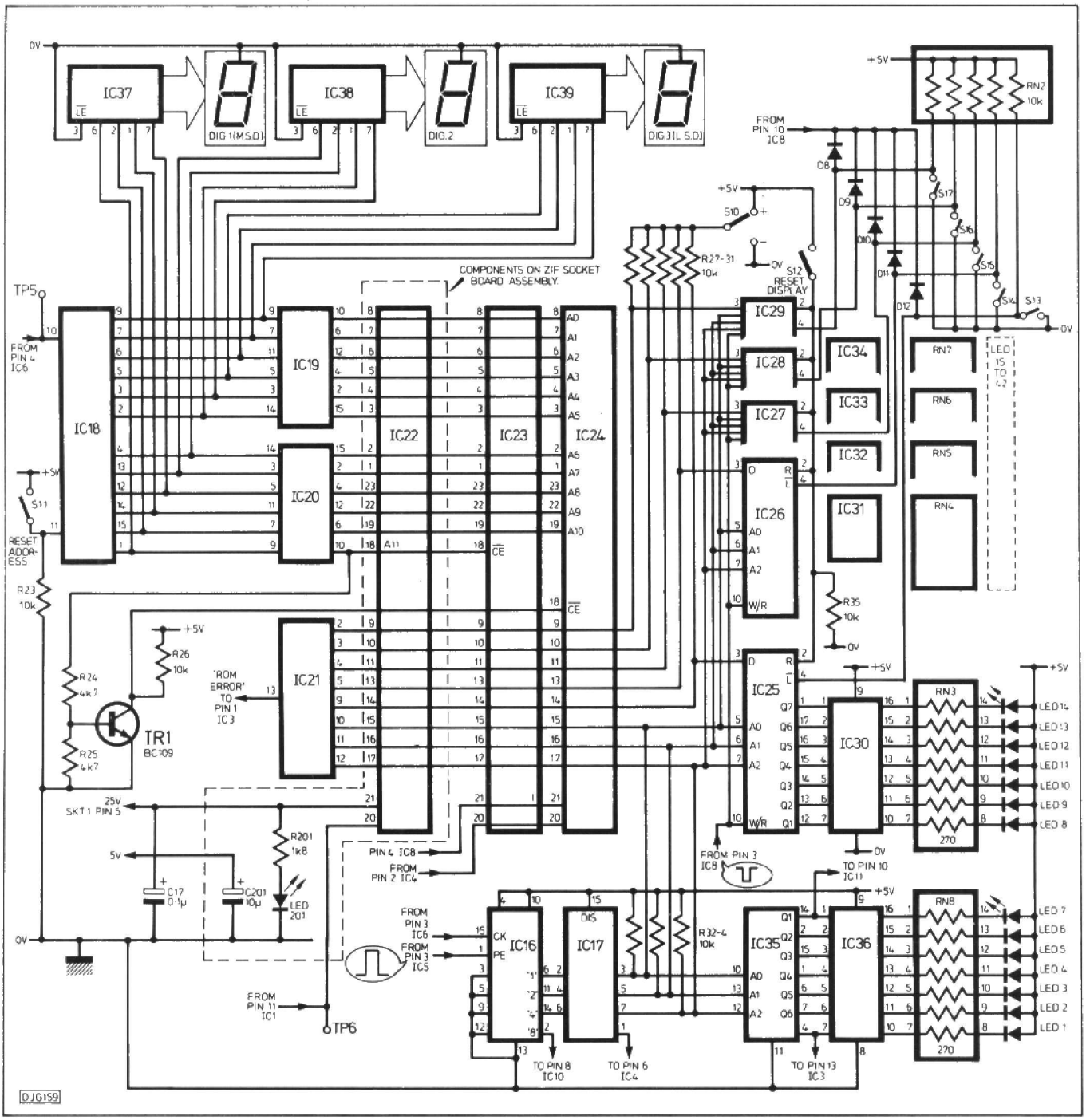


Fig.3. *Programme display circuit diagram.*

the Data in/out pin 3. Pressing one of the TOGGLE switches takes the corresponding LATCH pin, 4, low, this stores the data present on that latch input. Pin 10 of the latches is high at this point, through 8a/3, this is the W/R line, and determines the direction of data flow to the latches. When it is low the data is read from the latches.

Resistors R27 to 31 are not connected directly to the 5 volt line as you might expect, but to S10. Holding down a toggle switch, and pressing the +/− switch, S10, will take the data in to the latch low, and turn the lamp off.

The latches are 4599's, which comprise 8 separate flip-flops which are accessed through a BCD code on pins 5, 6 & 7. The contents of each of the latches is continuously available to drive the lamps, through buffers, IC30–34. From this it is apparent that only seven of the eight latches are needed, since only seven lines are used. The address BCD 000 is never used, and this latch is redundant in each of the five 4599's.

Pressing S8 triggers the MONO made up of 7c and 7d. This is needed to debounce the ROW switch, S8. The positive going edge of this is used to clock round IC16, a 4516 counter, the BCD outputs of which are taken to tristate buffer, IC17. This buffer is enabled by a low on pin 1, which is taken from the output of IC4c/6, and the BCD address for the latches is fed onto D5, 6 and 7 lines of the data bus.

At the same time they are also taken to IC35, a 4028, a BCD to Decimal decoder. This chip decodes the input, and outputs a high on one of ten lines. Again, we only use seven. These outputs go to a buffer, IC36, and to LEDs, this shows the ROW which is being addressed by the BCD bus to the latches.

So now we can select the ROW, TOGGLE the LEDs and make the data stored in the latches either +(ON) or −(OFF). Having decided that the correct lamps are lit it only remains to save onto the RAM, and this is done by pressing RAM PROG once.

Switch S6, RAM PROG puts a high onto 2d/13, and 2d/11 goes high since S7 is already closed. The output from 2d is differentiated by C1/R8 and caused bistable 11as, a 4013, to flip over, taking pin 1 high and pin 2 low.

Pin 1 going high sets a high on 8b/5, 8a/1 and 10a/1. Pin 2 going low blocks 2c, enabling the sequencer and starting the clock. The positive edge pin 1 is differentiated by C2/R11, and Presets the BCD address counter, IC16, to address 001.

As the Q2 output of the sequencer goes high, the output of 8a/3 also goes low via the OR gate, 9b, and remains so for three clocks counts, setting the W/R line low on the latches. This reverses the direction of the data lines to the latches, and they now place the latched data onto the bus.

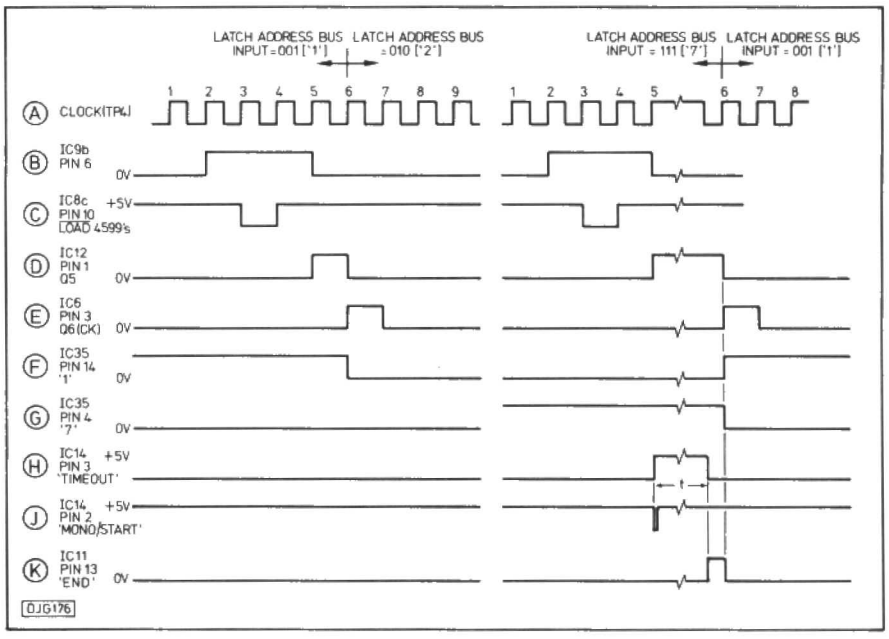


Fig.4. *Timing diagram*

When Q3 goes high 8b/4 goes low, and puts the RAM into WE mode, storing the five data and three address bits.

Q6 of the sequencer clocks the BCD and 4040 address counters by one, and the sequence is then repeated until the BCD counter reaches decimal '8', and pin 2 of IC16 goes high.

When this occurs pin 8 of 10a goes high. Two clock pulses later, that is, when Q8 goes high, the output of 10a goes high, resetting 11a, stopping the clock, resetting the 4017, and presetting the 4516 through C3/R10 and 5a. The BCD counter is preset merely for the sake of convenience, as it was found in practice that most new programmes are most easily written from the top down. The main address counter is not reset of course, otherwise the data just stored would be overwritten!

This is the recording sequence, and it is repeated, seven addresses at a time, to the maximum of 2046 addresses, giving almost 300 differents ets per EPROM.

Following the dumping of a few sequences onto RAM it is nice to have a replay of what you've just done, checking that there are no mistakes prior to burning it into PROM.

NEW switch, S7 is switched off, and RAM PLAY (obvious, ain't it?), is switched on. The 4040 address counter must be reset to 000, by closing S11 so that the programme runs from the beginning. IC2b/4 goes high, enabling the RAM output on pin 20, through the inverter 4. 6c/10 goes high, enabling gates 8c and 10b. The main system clock is allowed to run, and the sequencer starts clocking through.

Q2 and Q4 outputs do nothing, but Q3 clocks 8c/10 low. This is the LOAD lines on the latches, the same lines as were addressed separately during the TOGGLE sequence. They are all pulled low for one clock pulse through Diodes 8–12, and this latches the data through to their outputs.

The Q6 output of the sequencer clocks the 4040 round by one, and this sequence continues until the BCD address contained in the highest three bits of the bus is a 7 (111). When this occurs it is decoded by IC35, whose Q7 output will go high. This is taken to 3d/13. The sequencer had clocked this data through at the last Q6 output high stage, so 3d/11 remains low until the NEXT time Q5 goes high, that is 10 clock pulses later. Doing the timing this way round, dump data first and clock second allows address 000H to be used.

ANOTHER 555

Having reached the seventh byte and latched the data into the 4599s, Q5 of the sequencer goes high, and 3d/11 follows. This pushes 10b/6 high, and the leading edge of the pulse is differentiated by C11/R20, inverted by 7a, and fires MONI 1 (Yes folks . . . another 555 timer!). Pin 3 of the mono goes high, stopping the system clock for a time depending upon the setting of VR1. In this way the data from the seven addresses which has been latched into the 4599s is held, enabling the eye to register the display. The second part of IC11, a 4013, is clocked by the inverted output from the mono via 4a/2. The clock input of the 4013 is EDGE triggered, and at the end of the timing delay the Q output, pin 13 goes high. Provided the next BCD address in the data is a decimal 1 (001), which it will be during a sequence of recorded data, then the Q1 output of IC35 will go high and reset 11b via pin 10.

Playback of all the data will follow this sequence until the end of the recording is reached. What will happen

then is the system will detect a BCD 7, followed by another 7, and another and so on. This has the effect of triggering the mono every cycle, and bringing in the display delay.

During a replay sequence it is useful to be able to stop the clock at the end of the recorded data, ready to continue with the recording. Holding END closed takes 10c/12 high, the end of the display time out sets 10c/13 high, and when Q8 of the 4017 goes high the clock will be stopped by 10c, 9c, 9a and 4b. Then selecting NEW again will reset the sequencer, so that the first available empty address is used.

Should it be necessary, the 4040 address clock can be advanced one at a time by holding END closed and pressing S8, ROW. This is achieved through 3c and 6b.

The output data from the latches may be reset to all low by pressing RESET DISPLAY, S12. Unfortunately the 4599s can only be set one bit at a time.

When making up a program it is certainly worthwhile doing say a couple of dozen stores on RAM before checking and dumping onto PROM. The PROM PROG sequence is as follows.

Closing S1, ROM PROG and S2 RAM PLAY will start the programming sequence. S1 enables 3b, and blocks 7a, this prevents the mono being triggered.

MAIN CLOCK

The main clock is allowed to run and the 4017 runs as before. When Q3, pin 7 of the 4017 goes high a positive going pulse is differentiated from the output of 3b/4, by C6/R12. This short duration positive pulse is inverted by 4e, and triggers MONO 2 (can you believe, yet another 555??). It is this mono which produces the Programming pulse to the PROM, and it is most important that the output pulse length is carefully checked before attempting to blow a PROM. See below, setting up and testing.

As a result of the trigger pulse on pin 2 of the 555, the output pin, 3 goes high for 50mS. This positive pulse is used to stop the main clock via 9c/12, and programs the PROM on pin 20, via IC1d/11, TP6.

Before any data can be blown into the PROM it is necessary for the programming voltage to be applied to pin 21. In the case of the 2532 this VPP is 25 volts. It may be applied as a steady voltage, and not pulsed if you wish, and this is the method used here. Control of the VPP is by the ROM PROG switch, which feeds a high level out to the power supply through resistor R1. Should the VPP be applied without the 5v line, then the PROM can (AND WILL!) be damaged. Using the 5v line to enable the 25v line safeguards against this possible danger.

Exactly how the VPP is generated will be described later.

Taking pin 20 of the PROM low will either cause the PROM to output data to the bus, if VPP is at zero volts, or make it store data if the VPP line is as 25v. In this way the pinout is simplified. As the data are stored in each address, the LED display on the front will show what is being stored in sequence, since the unit is in RAM PLAY at the same time. This is a handy check that everything is going according to plan.

At the end of the recorded data all eight lines will go high, and since the clean prom is erased to all bits high anyhow, no harm will come to the unprogrammed bits. This is why it is advisable to clear the RAM before you start programming. It only takes 50mS to programme it in, but a lot longer to erase!

Adding more program to an existing PROM – for example, after getting back from the pub! – is done in the same way as described above, and the end of the existing data can then be easily detected with the END switch. Having stopped at the last recorded byte it is necessary to keep the END switch depressed until the NEW switch is closed, otherwise the clock will start up again.

When attempting to correct or change any seven bytes it is necessary to first identify the START ADDRESS of the particular bytes, and by running the Display Timer mono at a very slow speed halt the clock at the last good byte immediately preceding the error. Then all that is needed is to overwrite the locations where the error occurs. Sounds simple, but it does require a bit of thought. The clock is halted most conveniently by flicking over the NEW switch.

Applying the VPP voltage to the PROM turns on the LED mounted on the board next to the ZIF socket. This is as much to confirm correct operation as warn. The programming voltage is decoupled by C17 which should be a 35 volt tantallum.

The prom socket is a zero insertion force (ZIF) type, and is mounted on a separate piece of Vero board, connected to the rest of the system with a header and ribbon cable. On test it was found necessary to decouple the 5v supply to the PROM with a 10μF cap, this was because the ribbon cable was left fairly long, and the supply line was picking up noise, probably from the power supply. The address bus from the 4040 is decoded by three 7-segment display driver chips. These are 9368s, and are special in that they will decoce and display HEX (A, B, C, etc.), and contain on-chip constant-current output drivers, so limiting resisters are not required.

IC19 and 20 are not inverting buffers, type 4050. Address line A11 is used to enable one or other of the RAM chips. Transistor (do you remember them things? funny little fellas with three legs!), TR1 inverts the A11 line, which is fed to the $\overline{CE}$ input of the high order RAM, enabling it's output from address 800H to FFFH. I have had it suggested, and I hope it was a joke . . ., that my next publication should be '101 things you can do with a 555 on a wet Sunday afternoon', but I think this is too long a title!

THE POWER SUPPLY

Mains power is applied to a 0–9, 0–9 transformer, via a double pole switch, ganged with VR1. Both the primary and the secondary windings are fused, the secondary fuse being located on the supply board. It is a good idea to take the supply in to the unit through a special mains filter type input socket, this will reduce noise either coming in or going out of the circuit. Not a bad idea near high-power disco gear.

The low voltage output is rectified and smoothed in the usual way before being applied to a pair of TL497s. These devices are switch-mode subsystems, and require a minimum of external parts to provide a stepped up or down output. The only thing to watch out for is that the DC voltage applied to 14 does not exceed 15 volts WRT ground.

IC1 steps the input down to 5v. Resistor R1, which is made up of two in parallel, is the output current limit resistor, and C3 determines the timing of the switching. The 5 volt line has to be capable of delivering in the order of 750mA, but the 497 can only supply 500mA. To overcome this problem TR1, a P-Channel MOS FET is used as a current booster. R2 and 3 drive the FET well into saturation. L1 is a hand wound coil on a RS ferrite type RM10/400, and comprises 19 turns of 20swg en. cu. wire. Capture diode D1 is a special high speed type, designed for use in SMPSs. In case of problems in obtaining exactly the same type the PCB has been laid out so as to accept either a normal tubular style, or one of the T0 220 type of encapsulations. The output voltage is set up by adjusting VR1, and this should be done BEFORE ADDING ANY OF THE MEMORY CHIPS. The 5v line should be set to 5.1 volts, and no more. C4 is the usual smoothing cap on the output. The 25v line is a little more involved.

Next month – construction and testing of the Programmer Unit. PE

The parts list for the programmer will be published next month and the p.c.b. will be available from the PE PCB Service.

STE BUS

PART ONE BY RICHARD WHITLOCK

The Omnibus is here!

The use of the STEbus in industry is becoming extremely popular amongst firms requiring a versatile 8-bit processor system. It is expected to carry an IEEE standard in the near future making it the only 8-bit bus to do so. There is no doubt that STE is here to stay and will become extremely popular with designers and users alike. In this article we take a close look at all aspects of STE.

THE STE bus, soon to be the subject of a definitive IEEE standard, is, for users of 8-bit microprocessors, one of the most exciting and liberating developments in the whole fifteen year history of microcomputing. This may seem a wild claim but, as we explore the potential power, flexibility and sophistication of the concept, I think that most readers will come to recognise its truth.

The STE bus is the 8-bit realisation of a new conception of what a microcomputer system should be (the VME bus performs much the same function for users of microprocessors with 16-bit wide data busses). Most earlier multi-board microcomputers have been for all the world like a single-board design 'chopped up' into a collection of modules, some necessary and some optional, from which the user could assemble the facilities required for a given application. So far, so good: a flexible, economical approach. However, the limitations of the approach lie in the means by which the various boards are linked together: the bus. Mechanically and electrically reliable it may be, but adaptable it certainly is not. It will be based upon the control signal and timing characteristics of a particular family of microprocessors, and will present real problems to anyone who wishes to impose another family of micro-processors upon it. Take a look at a Z80 based S-100 system for example or, if you can find one, a 6800 based S-100. (The S-100 was designed with the 8080's most primitive status signals very much in mind.) The solution to the problem of making one microprocessor look like another takes a lot of logic and a lot of board space. STE tackles the problem of accommodating alternative microprocessors on a single standard bus by specifying its own set of control signals and signal exchange sequences, which any microprocessor can be made to imitate with relative ease.

With STE, the user will no longer be limited to the software base of a single microprocessor family. If some particularly attractive piece of software becomes available, then the appropriate microprocessor can be bought and slotted into the existing system. Power supply, backplane, memory and I/O will work just as well as ever with the new board. Similarly with hardware: if a new intelligent device controller becomes available on the STE bus, then it is universally available, not just to the owners of Shufflebus Z80 or 6502 systems.

Fig. 1 and Table 1 provide a condensed introduction to the signals used on the STE bus and the features provided by the system as a whole. A brief perusal of these will aid comprehension of the discussion below.

FUNCTIONAL ELEMENTS OF AN STE BUS SYSTEM

There are four functional elements involved in the STE concept.

A) The System Controller
B) The Bus Arbiter
C) Bus Masters
D) Slave sub-systems

A) The System Controller. Each STE Bus System has a single System Controller. The System Controller has three mandatory functions:

i) To generate the System Clock signal, SYSCLK. This is a 16Mhz, nominally square-wave, TTL level signal with the following timing specification:

Cycle time = 62.5 ns, +1 ns/−1 ns.
Clock High time = 31.25ns, +10 ns/−10 ns
Clock Low time = 31.25 ns, +10 ns/−10 ns

The backplane SYSCLK line is driven continuously by a conventional totem-pole buffer output for the whole time that the system is powered up.

ii) To generate an initial power-on reset signal for the whole system, SYSRST*, with a duration of between 200ms and 500ms, times being measured from the point at which the 5V V_{cc} supply reaches its minimum acceptable level of 4.875V. If the 5V supply subsequently falls below this minimum acceptable level then the system controller is required to assert SYSRST* for the whole of the time that the 5V supply is below specification. SYSRST* is driven by an open collector buffer.

iii) To monitor the data transfer handshake signals during every bus cycle and to generate the Transfer Error signal, TFRERR*, if, having once been initiated, the handshake process is not completed within a set time. This set time is required to be user selectable, the standard specifying only that the user shall be able to select a time of 8μs or less, in addition to longer periods which may be available. This stipulation is made to accommodate those micro-processors which have a limited bus cycle stretch capability. TFRERR* is driven by an open collector buffer.

If the necessary monitoring circuits are available, the system controller has a fourth, optional, function defined. If advance warning of a power failure is available more than 4μs before the 5V supply falls below 4.875V, then the following shut-down scheme should be followed:

a) Attention request 0, ATNRQ0*, should be activated immediately power failure is detected.

b) Over 2 millisecs later SYSRST* should be activated. The timing of SYSRST* is further defined to be at least 50μs before the 5V line drops below 4.875V.

This operation is of particular use where battery backed RAM is available to store vital data before SYSRST* becomes active, or where real-world controlled machinery may need to be left in a stable condition before control ceases. On the following power up, whether from 'cold' or at the end of a temporary power fluctuation, ATNRQ0* should be

Table 1.

IMPORTANT FEATURES OF THE STE BUS SYSTEM

A) MECHANICAL:	i)	Compatible with the 19-inch equipment sub-rack.
	ii)	Single or double eurocard sized boards and modules.
	iii)	IEC 603-2/DIN 41612 indirect connectors.
	iv)	Total position independence of logic boards and modules in the backplane.
B) ELECTRICAL:	i)	16MHz system clock.
	ii)	Terminated bus signal lines capable of supporting 200nS data transfer cycles.
	iii)	+5V, +12V, −12V and standby power supplies available, ready regulated, on the backplane.
C) LOGICAL:	i)	1Mb memory space and 4Kb I/O space addressable via the bus.
	ii)	Address valid signal.
	iii)	8-bit bidirectional data bus: asynchronous data. Transfers controlled by two line handshake.
	iv)	Transfer error signal to terminate accesses to non-responding addresses.
	v)	Multiple bus masters accommodated to a maximum of three fully independent systems.
	vi)	Eight prioritised attention request lines for user defined asynchronous status signalling: interrupt requests, direct memory access requests, error condition flagging etc.
D) SYSTEM GOALS:	i)	Bus operation completely independent of the specific characteristics of particular families of microprocessor and support components in all respects except overall bus cycle time.
	ii)	Total compatibility between boards from different sources adhering to the standard.

reasserted, or be still asserted, if logic functioning has not been lost, until the 5V supply is back above 4.875V. 200μs to 500μs later the SYSRST* signal may be removed.

B) The Bus Arbiter. The Bus Arbiter has a single simple function; to ensure that only one potential controller of the system bus attempts to use it at a time and further to ensure that the current controller has the use of the bus, without interference, until it has finished a number of complete data transfer cycles. The bus arbiter must ensure that each time a new device takes control of the bus, the signals imposed upon the bus lines by the previous controller have had time to disappear and the bus lines are in their rest states as dictated by the termination networks. To achieve this the bus arbiter inserts a delay of one SYSCLK cycle between one device quitting the bus and another being granted permission to put its signals on the bus.

Devices capable of controlling the bus to initiate data transfers are termed 'Masters' (see below). To obtain control of the bus, a master signals the bus arbiter by pulling whichever bus request line, BUSRQ0* or BUSRQ1*, is exclusively assigned to that master, low by means of an open collector buffer. This line then must remain pulled low until the master has gained control of the bus and made as many data transfers as required. In due course, when the bus arbiter has determined that the requesting master has the highest priority amongst competing requests and the necessary bus settling time has elapsed, the master is granted permission to gate its signals onto the bus. The bus arbiter does this by setting low the bus acknowledge line, BUSAKO* or BUSAK1*, exclusively assigned to that master and corresponding to the bus request line from that master, i.e. BUSRQO*/BUSAKO* and BUSRQ1*/BUSAK1*. From then on the master has exclusive control of the bus until such time as it allows its bus request signal to return high, whereupon the bus arbiter drives the corresponding bus acknowledge signal high and that master's bus control is over for the time being. Once its bus acknowledge signal has gone high again a master may apply for another period of control of the bus at any time.

There are only two pairs of bus request/bus acknowledge lines on the backplane, so how can the system accommodate three masters? If the bus arbiter shares a board with one master there can be a third pair of lines internal to that board which can function in exactly the same way as those on the backplane. It was stated above that the bus request/bus acknowledge signal pairs were each exclusively allocated to a single master. This will be the case in most systems where three masters or less are all that is required. However, in super-complex systems, it is permissible to attach a group of masters to each of the line pairs, provided that a system of intra-group signalling, using the attention request lines, is implemented, to ensure that only one of the group can request bus control at a time.

C) Masters. An STE master is any system element that has the capability of taking control of the system bus for the purpose of transferring data from one system element to another.

Typically a master will be a microcomputer in its own right, in the sense that it will consist of a microprocessor, ROM, RAM and I/O, in addition to an interface to the STE bus. This internal memory and I/O is directly addressable by the master's own microprocessor, without gaining control of the STE bus, and is not addressable by any other master, either directly or via the STE bus. Thus masters' microprocessors have a private sphere in which they can be programmed to work while they are not in command of the STE bus. In this internal space they will typically exhibit all their family peculiarities, operating as normal Z80s, 6502s, 8088s, 6809s etc, with all the variety of timing and control signals that this entails. However, when they address those parts of their memory maps which correspond to their interfaces to the STE bus, then their particular signals will be transformed, by the particular logic of their STE bus interface, into a single standard set of signals suitable for the STE bus lines and asynchronous signalling protocols.

Clearly the precise logic necessary to interface a particular microprocessor to the STE bus will, in general, be unique to that type or family of devices. For this reason the STE bus signalling protocols are defined in terms of sequences of events with few intervening time intervals specified. A few minimum intervals are specified where the signal propagation and settling delays of the driver-connector-backplane-connector-receiver complex demand attention. A few maximum intervals are specified at the end of a bus cycle, when cancelling active signals and generally clearing the bus of redundant information are important. On the whole the standard is permissive rather than restrictive and there will be many, more or less efficient, ways of transforming a given microprocessor's native signals into STE standard forms.

Now we know roughly what a master may consist of internally and we have examined the essentials of how it acquires control of the STE bus. It must be obvious that there must be a great deal more to the business of sharing the STE bus amongst a number of masters to create an efficient system. As things stand, the first master to be awarded the control of the bus could 'hog' it for ever.

Fig. 1.

THE STE BUS SIGNALS

CONNECTOR PIN ROW 'a'				CONNECTOR PIN ROW 'c'			
Ground		0V	1	0V	Ground		
V_{cc} Regulated supply		+5V	2	+5V	Regulated supply V_{cc}		
Data Line 0	(3S) (M&S)	D0–LSB	3	D1	Data Line 1	(3S) (M&S)	
Data Line 2	(3S) (M&S)	D2	4	D3	Data Line 3	(3S) (M&S)	
Data Line 4	(3S) (M&S)	D4	5	D5	Data Line 5	(3S) (M&S)	
Data Line 6	(3S) (M&S)	D6	6	MSB–D7	Data Line 7	(3S) (M&S)	
Address Line 0	(3S) (M)	A0–LSB	7	0V	Signal return Guard track		
Address Line 2	(3S) (M)	A2	8	A1	Address Line 1	(3S) (M)	
Address Line 4	(3S) (M)	A4	9	A3	Address Line 3	(3S) (M)	
Address Line 6	(3S) (M)	A6	10	A5	Address Line 5	(3S) (M)	
Address Line 8	(3S) (M)	A8	11	A7	Address Line 7	(3S) (M)	
Address Line 10	(3S) (M)	A10	12	A9	Address Line 9	(3S) (M)	
Address Line 12	(3S) (M)	A12	13	A11	Address Line 11	(3S) (M)	
Address Line 14	(3S) (M)	A14	14	A13	Address Line 13	(3S) (M)	
Address Line 16	(3S) (M)	A16	15	A15	Address Line 15	(3S) (M)	
Address Line 18	(3S) (M)	A18	16	A17	Address Line 17	(3S) (M)	
Bus Cycle Type = R/W*	(3S) (M)	CM0	17	MSB–A19	Address Line 19	(3S) (M)	
Bus Cycle Type See Text	(3S) (M)	CM2	18	CM1	Bus Cycle Type + Mem/IO*	(3S) (M)	
Address strobe	(3S) (M)	ADRSTB*	19	0V	Signal return Guard track		
Slave handshake	(OC) (S)	DATACK*	20	DATSTB*	Master handshake	(3S) (M)	
Transfer error	(OC) (C)	TFRERR*	21	0V	Signal return Guard track		
Attention request	(OC)	ATNRQ0*	22	SYSRST*	System Reset Signal	(OC) (C&M)	
Attention request	(OC)	ATNRQ2*	23	ATNRQ1*	Attention Request	(OC)	
Attention request	(OC)	ATNRQ4*	24	ATNRQ3*	Attention request	(OC)	
Attention request	(OC)	ATNRQ6*	25	ATNRQ5*	Attention request	(OC)	
Signal return/Guard track		0V	26	ATNRQ7*	Attention request	(OC)	
Bus access request	(OC) (M)	BUSRQ0*	27	BUSRQ1*	Bus access request	(OC) (M)	
Bus access grant	(TP) (A)	BUSAK0*	28	BUSAK1*	Bus access grant	(TP) (A)	
16 MHz system clock	(TP) (C)	SYSCLK	29	+VSTBY			Battery or V_{cc} as required
Auxiliary supply, reg'd		−12V	30	+12V			
V_{cc} regulated supply		+5V	31	+5V			Regulated supply V_{cc}
	Ground	0V	32	0V	Ground		

* = Active low signal, i.e. true when pulled low, false when high or not driven.

KEY
LSB = least significant bit; MSB × + most significant bit;
First bracket shows type of line driver used; TP = totempole, OC = open collector, 3S = three state.
Second bracket shows source(s) of signal; A = bus arbiter, C = system controller, M = master, S = slave.

In fact, we have so far only hinted at the existence of a bus arbitration algorithm and implied only one mode of bus tenure on the part of masters. The alternatives that can be implemented in combinations of hardware and software within the STE standard are much more complicated and flexible than this.

Take the case of a system with two masters. The simplest possible approach would be for each master to take control of the bus for arbitrarily long periods, as and when its requests were granted. The bus arbitration algorithm could be a simple priority scheme. If two requests arrived in the same time slot then the master on BUSRQ0* would be given priority over the one on BUSRQ1*, otherwise each new request would have to wait for the other master to finish. Each master would be operating in a 'release-when-done' mode. Given a degree of software discipline this scheme can work well in a wide variety of situations.

RELEASE – WHEN – DONE

Suppose now that one of the masters was engaged in an application that required short, regularly spaced, periods of bus control. Examples could be some sort of machine control or data logging. Now it would be better if the master so engaged could somehow signal to the other master to get off the bus, briefly, in the event of both requiring access simultaneously. An attention request line could be used to interrupt the latter master's microprocessor or to set a flag which the latter master polled regularly. Thus the master with a tight schedule could get control of the bus quickly as and when it needed it. In this case the master with the regular access requirement could operate in the simple 'release-when-done' mode while the other master would be operating in 'release-on-request' mode. In this case the 'release-when-done' master would make its requests to the bus arbiter via the higher priority BUSRQ0* line, so as to be awarded bus control in the event of both requests coming in the same time slot.

Note that the bus arbitration algorithm, probably embodied in hard wired logic, is identical in both the above cases. Considerable flexibility can be accommodated by reprogramming masters' software and perhaps relocating a few jumpers on masters' boards. If this is still insufficient then a more complicated bus arbiter can be used, as there is no restriction placed upon the nature of the bus arbitration algorithm by the STE standard. Rotating priority schemes, sequential access schemes etc are permissible if they meet the needs of a particular application.

A common factor in all the foregoing discussion is that at power up the bus is in the hands of the bus arbiter and subsequently no master acquires control of the bus without requesting it, and possibly having to wait for a period. In the case where a master shares a board with the bus arbiter, not only can there be three-master bus sharing in all the ways touched on above, but a new possibility is opened, that of a 'default master'.

A default master has control of the bus whenever no other master has been granted control. Thus it automatically has the lowest priority for bus control. When the bus is otherwise free, the default master is able to place its signals on the bus whenever necessary but, when a bus request from another master is received by the bus arbiter, the default master must be somehow driven off the bus until it is again free. How this is done will depend to a great extent on which microprocessor is at the heart of the default master. It may be stopped,

totally, at the end of its current or next instruction cycle by asserting a HALTor DMARQ type signal, the resulting acknowledge signal being taken as clearance to transfer bus control to the requesting master. Its clock may be stopped at an early stage of the next instruction cycle, before any timing signal edges of use to the STE interface logic have occurred. There are a multitude of methods applicable to different devices. If the default master is addressing internal memory and I/O at the time that the bus request arrives, it may even be possible to let it run until it tries to use the STE bus. The common factor in all these approaches is that they all require signals other than BUSRQ* and BUSAK* to be exchanged between the default master and the bus arbiter. These signals are not provided for on the backplane and so default master and bus arbiter must share a board.

Finally, on masters, it is the responsibility of logic internal to the master to generate the appropriate local reset signals in response to SYSRST* and masters are permitted to hold SYSRST* low for additional periods of time to perform internal diagnostics if required. During the assertion of SYSRST* Masters may request bus control, and the bus arbiter may grant it to one or another, but no signals may be put onto the bus until SYSRST* is released.

It is this latter type of secondary processor that is becoming extremely important in STE terms. Typically they interface to the STE bus as a few I/O ports to which the STE masters write quasi-high level instructions or data to be processed and from which they read status information or result data. This is the limit of these slave systems' interactions with the STE bus. Internally however they may be extremely complex, amounting to microcomputers as powerful as any master.

This delegation of time consuming functions to secondary processors has a number of important consequences for the whole system. The demands on bus time are reduced since now a few bytes of coded instructions transferred may be the equivalent of frequent reads and writes to 'dumb' I/O devices. Master microprocessor time is also freed, allowing more complicated supervisory tasks to be undertaken in real time. Finally, and perhaps economically the most important, master programming is simplified and speeded, since, in most cases, high-level languages will run fast enough for the most demanding tasks, without recourse to machine-coded segments.

Of course a wide range of 'dumb' and semi-intelligent I/O devices and peripheral controllers are available for less demanding and more cost-critical high volume applications.

D) Slaves. Memory and I/O port arrays which are capable of being controlled, i.e. written to and read from, by masters via the STE bus, are termed slaves.

This sounds very pedestrian in comparison to our earlier discussions. Certainly ROM and RAM are much the same in any system, but I/O for the STE bus is rapidly becoming something else! With the large potential markets for boards with the standardised interface to the STE bus, manufacturers are really getting stuck into intelligent I/O processors. Today almost any CPU-time intensive task can be delegated to a secondary processor. Examples range from the more or less integrated floating-point arithmetic co-processors, which can greatly enhance the computational speed of recently introduced micro-processors, to devices like intelligent stepper motor controllers, based upon general purpose single-chip microcomputers. PE

PART TWO – NEXT MONTH – STE READ AND WRITE CYCLES

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Design ideas and circuit elements for true hi-fi.

VIDEO FADER ★
Following from this month's Video Enhancer, we have another super project for video enthusiasts. This is a cost effective approach to video mixing allowing simple fade-up and fade-down functions.

★ **DEAF ALARM**
Deafness or partial hearing is suffered by thousands of people and it's no joke. This project is a simple alarm-clock add-on which provides an effective alarm for the deaf.

Plus all our regulars including circuit ideas for Ingenuity Unlimited, Micro Forum, and News and Market Place.

WE HAVE A BRILLIANT EDITORIAL FEATURES PLAN LINED UP FOR NEXT YEAR INCLUDING REGULAR DESIGN AND TECHNOLOGY FEATURES, MICROFORUM FOR ALL HOME MICROS, EXPERIMENTAL ELECTRONICS AND SOME GREAT CONSTRUCTIONAL PROJECTS

ON SALE FRIDAY DEC. 5th 1986

PROFESSIONAL FRONT PANELS

BY 'THE PROFESSOR'

Go-faster stripes for electronic constructional projects!

Practical Electronics is traditionally a magazine for the serious experienced constructor. However, many of the projects featured are attracting newcomers to the hobby—especially those from the world of computers. Over the next few months, the 'prof' will be describing a range of useful tips and techniques for all hobbyists from novice to professional.

It is probably true to say that with most projects the electronic side of construction is the easy part, and it is dealing with the mechanical side of things and getting a professional looking finish that represents the biggest hurdle. Using a ready made printed circuit board or a home constructed type produced with the aid of rub-on transfers it is fairly easy to obtain really neat results, but with the external finishing things tend to be more difficult. While a high standard of finish will not make a project perform any better, proud hobbyists should strive for the best possible finish. It would be a mistake to let high quality exterior finish become the primary aim with little attention being paid to the standard of electrical construction (which would be comparable to the hi-fi fanatics who only hear the quality of reproduction and not the music), but producing a neat finish is a worthwhile and rewarding aspect of construction.

PHOTO-PANELS

Most modern cases have a high quality of finish, and it is the panel legends that largely determine whether a project looks home-made or like a commercially produced product. Good results can be achieved by applying rub-on transfers direct to the case, but standard of finish does not compare with that of most ready made equipment. Many readers will be aware of photographic methods of front panel production, but the exact way in which these are produced is less well known. It is actually a much more simple process than one might think, and it is not essential to have any special or expensive equipment. It is certainly something that is within the capabilities of most electronics hobbyists. Results with even a very small and simple panel design are really first rate, and the effect is something that really needs to be seen 'in the flesh' in order to fully appreciate it. A common complaint about panels finished with rub-on lettering is that the letters are easily chipped, and spraying on a protective coating only partially alleviates the problem. For reasons that will become apparent later, this problem is completely overcome when using photographically produced front panels, which are very durable indeed.

When producing a panel the first requirement is for a 'master' from which the photographic copy can be made. This is normally made from rub-on transfers applied to drafting film, and the latter is available from some of the larger component retailers. It is sold as an aid to printed circuit production, but is equally valid in this application which has strong similarities to simple methods of photographic printed circuit production. Single mat, double mat, and transparent types are all suitable, although the double mat variety is probably the easiest to use. Tracing paper is also usable, but it is less stable than proper drafting film and might give slightly less accurate results.

What is probably the easiest way of doing things is to draw out the required front panel design on paper, and to then fix the drafting film over this so that it can be easily and precisely copied. With a case that has a removeable front panel it is possible to mark the design onto the panel itself, and to then fix the drafting film over the panel for copying purposes.

A wide range of letter styles and types are available these days, and there are also lines and various symbols available which can be used to good effect. A point to bear in mind is that the final panel is a negative of the master, and black lettering on a clear background becomes clear lettering on a black background. The colour of the letters is determined by a backing paper which can be white or one of several colours. In fact it would be feasible to patch together a backing made from several different colours to produce multicoloured lettering, but it is difficult to envisage many projects where the gaudy result would be desirable.

If a largely black panel is not required, areas of the master can be covered over with drawing ink (or any other strong ink) so that these areas appear as the background colour on the final panel. An alternative is to use a double negative system so that the final panel is a positive of the master, or to produce a master that is a negative of the required panel design. The latter would be very difficult to produce in practice, and making a negative copy of the master and then using this to produce the final panel is the more practical approach. However, this is something I have not yet tried, and results obtained using the single negative method are perfectly adequate for most purposes.

Rub-on transfers are not the only way of producing the master, and something like a simple computer drawing package and a plotter or printer can give good results, as will anything that can produce a reasonably opaque design on drafting film or tracing paper.

EXPOSURE

The film is a slow type which is only sensitive to ultraviolet light. It can therefore be exposed to ordinary daylight without becoming fogged, but it should be stored under dark conditions and it should not be subjected to direct

sunlight. A darkroom and safety-light are totally unnecessary. Ideally the film should be exposed in an ultraviolet exposure box, and inexpensive units of this type are available from a few components retailers. The film is exposed in the manner shown in Fig. 1 (the sensitive side of the film is the semi-mat side incidentally, and the plain side is the one with the high gloss finish). The master should have markings to show the limits of the panel (a dot to indicate each corner is sufficient) and the film should be trimmed down to size prior to exposure. It is tempting to simply leave the film over-size, and then precisely trim it down to size once it has been fixed in position. The problem with doing this is that it would be difficult to precisely position the finished panel, and a more practical alternative would be to cut the film just marginally over-size, and then do the final trimming once it has been fixed in place.

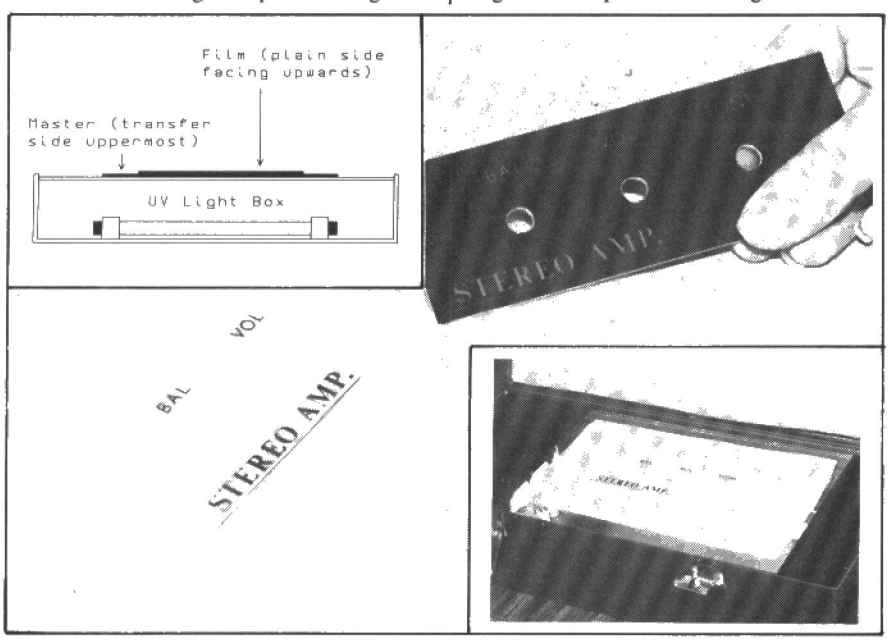
Ultraviolet light boxes, even the more simple types, are not particularly cheap, and few constructors will be prepared to buy one especially for producing front panels. An alternative is to put together a simple device which holds the master and film in place against a sheet of clear plastic or glass, and to use sunlight as the light source. The problem with this method is that it is impossible to accurately control the exposure, and this would almost certainly result in a certain amount of wasted film. With an ultraviolet light box the recommended starting points for exposure times are 45 seconds for a 120 watt box and 90 seconds for a 32 watt type. The optimum exposure time depends on factors such as the distance from the tubes to the film, and how well or otherwise the drafting film or tracing paper used for the master allows ultraviolet light to pass through to the film. With any photographic process of this type over exposure is always preferable to under exposure, especially if the design on the master is produced using materials that are well and truly opaque. With a 16 watt light box and double mat drafting film I found that an exposure time of 5 minutes gave good results. Direct sunlight requires a comparable exposure time.

DEVELOPMENT

For development two plastic trays are required; one containing sufficient developer to cover the film easily, and the other containing water. The film is immersed in the developer for ten seconds, and then it is removed and placed onto a paper towel with the sensitive side uppermost. The use of photographic tongs is recommended when handling the film as the softened emulsion is easily damaged. A pad soaked in developer is then used to gently wipe away the exposed areas of emulsion. No more than gentle wiping should be used or all the emulsion might be removed. If necessary the film can be returned to the developer for further development, but this is not usually necessary.

Once the unwanted emulsion has been removed the film is rinsed in the tray of water and carefully wiped with the pad to remove residues. The film can then be dried with a paper towel or even using a hairdrier, but it seems to dry quite rapidly if just left to dry naturally.

Inspection of the completed film will often reveal scratches or small spots where the emulsion has been removed. These can easily be filled in using a technical pen or any pen which has good black ink and is capable of marking onto the plastic backing of the film.



Permasign panel making kits and materials plus Alfac transfers are available from Verospeed, Stansted Road, Boyatt Wood, Eastleigh, Hants SO5 4ZY.

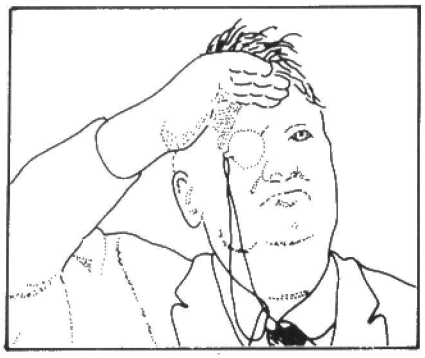
Even quite large blemishes can be invisibly mended in this way, and very minor blemishes are unlikely to show when the film is fixed in place. The film can be placed against a sheet of white paper for inspection purposes, and any imperfections which fail to show up when trying this will not be visible on the finished panel.

FINALLY

The final process is to fix the film in place on the case. It is glued in place using a laminate which is self adhesive on both surfaces. It is white on one side and either red, blue, green, or yellow on the other. Either the white or coloured side can face outwards, depending on whether white or coloured lettering is required. Clear material is also available, for use where the natural finish of the case must show through. This should be quite effective on aluminium and brushed aluminium effect panels.

Probably the best way of fitting everything in place is to first remove the backing paper from the laminate, then fix the laminate in position, trim it precisely to size using a modelling knife, and finally remove the front layer of release paper so that the film can be pressed into place. The adhesive is extremely powerful, and this makes it imperative to have the film accurately positioned before starting to press it into place. If it has to be removed it is likely to be damaged to the point where a new copy has to be made. Once it is in place any final trimming to size can be carried out. The manufacturers recommend that the film should be fixed to the laminate, and that the two should then be fixed to the case. I found this to be a more awkward way of doing things, but it might be preferred by some constructors and would be worth trying.

The film is placed emulsion side down, leaving the plain side with its high gloss finish facing forwards. This largely accounts for the high quality of finish obtained, and it also means that the lettering is protected by a tough layer of plastic which renders it virtually chip- and scratch-proof. At first there may be a mottled effect on the lettering, but this clears of its own accord in a few hours. If a mat finish is preferred to the natural gloss finish of the film, spraying with a clear mat finish lacquer will have the desired effect. PE



SPACEWATCH

BY DR PATRICK MOORE OBE

Our regular look at astronomy

The weather looks good on Mars – with blue skys? What is the explanation for the temporary holes which appear in the upper atmosphere?

NON-TECHNICAL TRIBUTE

IT IS sad to record the death of a man who was not technically an astronomer, but who made notable contributions in popularizing astronomical knowledge. Chesley Bonestell, the great 'space artist', has died at the age of 98. He was trained as an architect, but later made his reputation by his book illustrations, beginning with *The Conquest of Space,* written by Willy Ley – one of the original German rocket pioneers. Later, Bonestell collaborated with Ley and with Werner von Braun, who went to the United States after the defeat of Germany and master-minded the launching of the first American satellite, Explorer 1.

Bonestell's pictures of planetary surfaces as he believed them to be have been shown to be remarkable in their accuracy; only now and then can it be seen that some of the necessary scientific

"the sky is blue"

knowledge was not then available – as when Mars was given a blue sky! But quite apart from his superb artistic skill, he took immense care with his detail, and he set a trend which has inspired many later artists, of whom the latest to achieve world fame is Paul Doherty.

There is still considerable discussion about how to explain the observation of temporary 'holes' in the upper atmosphere, shown by ultra-violet images of the airglow taken by the US satellite Dynamics-Explorer 1, where the emission strength drops suddenly to only a few per cent of its normal value. Each area lasts for less than three minutes, covering an area of 1000 square miles. L. Frank, J. Sigwarth and J. Craven, of Iowa, attribute these 'holes' to the impacts of miniature comets, made up of what they call a fluffy frozen-water aggregate impacting at some 25 miles per second. The Iowa scientists

The Sky This Month

ONCE more this is not a particularly favourable time for planetary observers. Venus passes through inferior conjunction on 5 November, and by the middle of the month has become visible low above the south-eastern horizon before sunrise; Mars and Jupiter, both in Aquarius, are to be seen in the south-west during the evenings, but are past their best for this year (Mars has declined to magnitude 0.1), and Saturn is out of view altogether. This leaves us with Mercury, which is a morning object low above the south-eastern horizon late in November. On the 13th it will pass in transit across the Sun's face, though unfortunately this phenomenon will not be visible from Britain.

The only planets closer to the Sun than we are, are Mercury and Venus. Therefore, there must be times when they are lined up with respect to the Sun, so that they appear as black disks slowly crossing the Sun's face. During the transit, Venus is large enough to be visible with the naked eye, but it is not likely that there is anyone now living who has seen a transit; the last was in 1882, the next will not be until 2004. But transits of Mercury are less uncommon, and are interesting to watch, though optical aid is needed. They can occur only during May and November; the last before this month's was in 1973, while the next will be on 16 November 1993 and 15 November 1999. They are not rapid, and Mercury takes several hours to cross the solar disk. On 13 November, the transit will begin at 01.43 GMT and end at 06.31, so that it will be visible from Australia, Asia, part of Antarctica, Africa (except the north-west) and Eastern Europe.

The first transit of Mercury to be observed was that of 7 November 1631, which had been predicted by Johannes Kepler and was observed by the French astronomer Pierre Gassendi. On 7 November 1677 Edmond Halley, of comet fame, watched a transit from the island of St. Helena, where he had gone to study the southern stars, and later he suggested that transits might be used to measure the length of the astronomical unit, or Earth-Sun distance. His method was sound enough in theory, and was actually used for transits of Venus, which are much easier to study than those of Mercury, but the whole principle is not obsolete, so that modern transits are of no more than academic importance.

However, this month's phenomenon is interesting, and anyone who is able to observe it may care to try some photography – remembering, as always, that it is dangerous to look directly at the Sun, so that the only really safe method is to project the solar image on to a screen held or fixed behind the eyepiece of the telescope. It will be noticeable that Mercury will look much darker than any sunspots which happen to be visible.

The 'summer triangle' of the brilliants stars Vega, Altair and Deneb is still to be seen, though Altair is dropping toward the horizon by mid-evening. In the south the Square of Pegasus is dominant; look too for the bright star Fomalhaut in Piscis Australis (the Southern Fish), which is well south of the celestial equator and is always low even in Southern England, while in North Scotland it barely rises. Ursa Major, the Great Bear, is at its lowest in the north, which means that the 'W' of Cassiopeia is close to the zenith or overhead point; but midnight Orion is coming into view in the east, preceded by Taurus (the Bull) with the red star Aldebaran and the lovely star-cluster of the Pleiades.

The Moon is full on 16 November, which will not be welcomed by meteor observers – because the 17th is the maximum of the Leonid shower. The Leonids are notoriously erratic. Sometimes, as in 1966, they can provide magnificent displays, while at other times hardly any meteors from the shower can be seen. There is no reason to expect anything spectacular this year, but meteor observers will certainly be on the alert during the early hours of November 17, and they would much prefer the Moon to be out of the way!

develop their theory so as to explain the traces of water vapour in the atmosphere of Venus, and also the liquid which may once have flowed along the riverbeds of Mars. The theory has met with a little support, but it does seem that a 'rain of mini-comets' would produce far too much water to be in any way plausible, and few astronomers take the idea at all seriously.

The two Russian Vega probes, which bypassed Halley's Comet a few days before Giotto did so, went to their target by way of Venus, and dropped balloons into the atmosphere of that peculiar planet. They floated at around 33 miles above the surface, which is near the top of the thickest part of the cloud layer, and continued to transmit for almost 50 hours, moving at an average speed of from 150 to 155 mph. Vega 1 registered a temperature 12 degrees higher than that of Vega 2, though it was at the same height, so that clearly there are definite variations inside the planet's atmosphere. There are also unexpectedly strong upcurrents and downcurrents. Both probes dropped landers onto Venus's surface; no cameras were carried on these occasions, but soil analysis was undertaken, and everything indicates that the evolution of the surface has been dominated by vulcanism. Vega 2's analyzed sample of surface material seems to contain four to five per cent of sulphur by weight, though there is admittedly a chance that there may have been reactions with atmospheric gases to produce a thin sulphur-rich layer over some other variety of rock.

THE LATEST ON MILLISECOND PULSARS

Pulsars have caused theoretical problems many sleepless nights ever since their unexpected discovery nearly two decades ago. However, there seems no doubt that they really are rotating neutron stars, the remnants of Type II supernova explosions. Until fairly recently the quickest spinner was the pulsar in the Crab Nebula, which had a period of $^1/_{30}$ of a second; this fits in well with the idea that the Crab is the youngest known pulsar – it is unquestionably the remnant of CN Tauri, the supernova observed in the year 1054. The detection of a pulsar spinning at 642 revolutions per second was quite unexpected. Since then two more 'millisecond pulsars' have been found, one of which has a period of 163 revolutions a second and the other (PSR 1855 + 09) 186 revolutions a second – in other words, 5.36 milliseconds.

It looks as though these ultra-fast pulsars are different from the older types. Since pulsars appear to be slowing down by tiny but measurable amounts, the millisecond pulsars cannot be very old if this is the only mechanism involved; in fact they do not seem to be slowing down at all. Assuming that they *are* neutron stars, we must deduce some way of keeping them 'wound up', so to speak.

The second millisecond pulsar was found to be a binary system, presumably with a Main Sequence star, or at least something much less evolved and condensed than a neutron star, associated with its pulsar companion. If the pulsar is pulling material away from the other star, and this material arrives at an angle, it may prevent any measurable slowing-down: in fact, quite the reverse; it may speed up the pulsar's rotation.

The new millisecond pulsar, PSY 1855 +09, has now also been found to be a member of a binary system, and this lends support to the hypothesis. On the other hand, it is certainly difficult to visualize a body the size of a neutron star – at least several miles in diameter – rotating at such a speed; even with the amazing density of neutron material, the star cannot be very far from being in danger of disruption. Altogether the millisecond pulsars are very strange objects indeed, and as yet we cannot be confident that our explantion of them is really satisfactory.

PE

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MICRO FORUM

ALAN TREVENNOR

Simple Z80 single stepper circuit

THE Z80 microprocessor is to be found as the central processor in top selling Amstrad and Sinclair home computers (to name only two). One of the most interesting uses for such home micros is developing firmware for single board application systems. The major problem comes with debugging such firmware, since address conflicts often arise which prevent debug on the mother machine. The circuit to be described here is a simple single stepper for Z80 application systems. Many previous circuits have been published, but this one has the virtue of simplicity and cheapness. The single step facility provided allows the use of a meter to ascertain the state of each address or data line before going on to the next instruction.

Fig. 1 shows the circuit in block diagram form. The Wait bar signal is an input to pin 24 of the Z80. Wait bar freezes the Z80 when it it pulled low. The M1 bar signal is an output from pin 27 of the Z80 which goes low to indicate that the MPU is fetching the first byte of an opcode. There are a number of Z80 multibyte opcodes for which M1 will go low several times. These are the opcodes which have a first byte with a Hex value of CB, DD, ED or FD. If desired link LK1 can be used to make the Z80 halt at every Read or Write using RD bar or WR bar. Note that M1 bar is also used in conjunction with IORQ bar to signal interrupt acknowledge. One further point to note is that if you are using the Z80 transparent refresh feature for dynamic memory in your application system this method of single stepping will be unsuitable, since when the MPU is halted the refresh feature also stops. The circuit is suitable for systems using static memories like the 6116 or 6264.

Referring to Fig. 1 the circuit consists of three blocks. The first block is a NAND latch whose output controls the state of the Wait bar line into the Z80

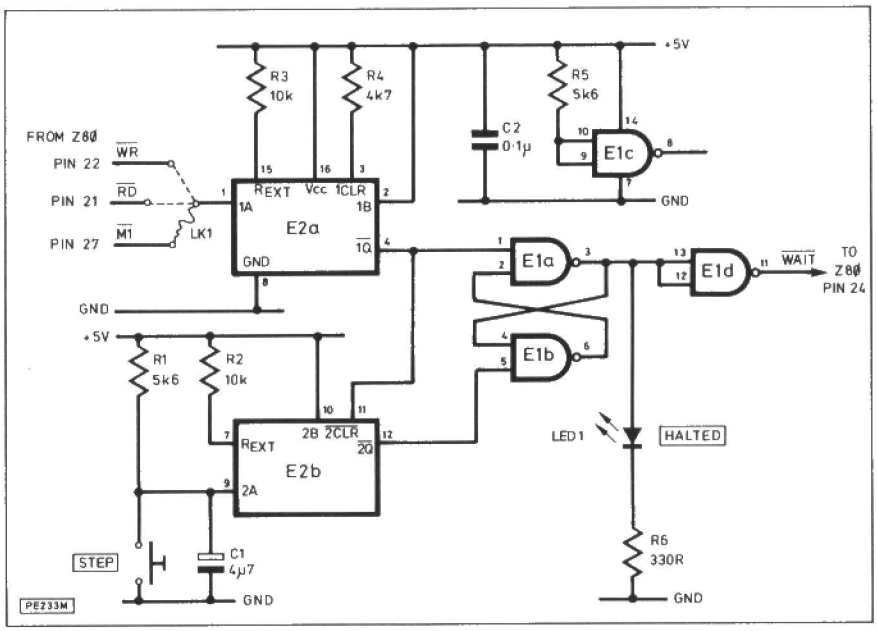


Fig.1.

and therefore commands run or freeze. The other two blocks are monostables which deliver pulses to set or reset the latch. The monostable which sets the latch to enable the Z80 to run is triggered from the Step push button, while the monostable which resets the latch and therefore freezes the MPU is triggered by whichever signal from the Z80 is selected using link LK1. The user can select M1 bar, RD bar, or WR bar as the stop signal source. Readers may like to modify the design to freeze the Z80 when a particular device is addressed, by connecting its CS bar line into this circuit.

Fig. 2 is the circuit diagram of the stepper. The selected stop signal source is fed into the negative tripper input of E2a. Triggering this monostable pulses pin 4 low which sets the NAND latch formed by E1a and E1b, and makes pin 11 of E1d go low – thus stopping the Z80. Also when a stop pulse is issued to the input of the latch the CLR bar input of E2b is pulsed low, ensuring that the monostable has an inactive output. When monostable E2b is triggered by pressing the STEP button its pin 12 pulses low, resetting the NAND latch and enabling the Z80 to run again. The capacitor and resistor R1 and C1 help to debounce the push button which should preferably have a snap action. On power-up the stepper will stop the Z80 at address zero if RD bar or M1 bar are selected as the stop signal source; if WR bar is selected the MPU halts when it first tries to write to the memory or I/O address spaces. E2c remains unused and could be used to invert high going stop signal sources. If unused, its inputs (pins 9 and 10) should be connected to +5 volts via a 5K6 resistor as shown. This will improve the noise immunity of the rest of the circuit.

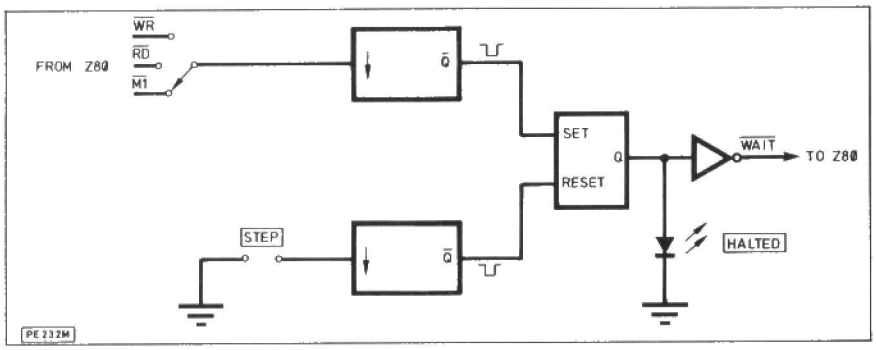


Fig.2.

If it is desired to have the facility to stop the Z80 in mid program, this can easily be accomplished by the addition of a normally closed switch connected between ground and the pin 3 side of resistor R4. This holds E2a in reset so that the NAND latch can never be set by the selected stop signal. When the Z80 is to be stopped, the switch is opened and the next incoming pulse to pin 1 of E2a stops the Z80 as before. This is useful where you need to stop a program which appears to hang up in the middle. PE

MICE AND ROBATS

REPORT BY JOHN BILLINGSLEY

at the Institution of Electrical Engineers, earlier this year

As reported earlier this year, the IEE is the official host to the Micromouse contest and John Billingsley an active "mouser" reports on the latest battle in London. The final was both entertaining and interesting with a line up of 12 runners.

AN ASSORTMENT of strange contraptions cluttered the hallowed Council Chamber of the Institution of Electrical Engineers as contestants readied their machines for action, thirteen mice and four ping-pong playing robots. Ever since the contest came to Britain, the Chairman of the IEE's Computing and Control Division has had the duty of Judge. Now the IEE has officially adopted the role of annual host to the contest.

A notable newcomer was David Otten's MITee Mouse from Boston, trying its wheels for the first time in serious competition. Otten's pilgrimage to the contest was beset with difficulties; on top of an eighteen hour delay in his flight, a four hour holdup by British Rail threatened to make him miss the contest. But it was all seen to be worth the effort when MITee, as guest contestant running first, put up a time of 1 min 44 seconds followed by one of the 36 seconds, scoring 32.37 points.

"I would have liked to beat it by a lot more"

The new scoring scheme was in use. To the time from starting square to centre is added two seconds per minute of elapsed 'appearance time', less ten seconds if the mouse has run to and from the centre entirely untouched until the scoring run is made. The scheme was entirely successful in deterring trackside fiddling. Most contestants achieved their best scores well within fifteen minutes, and by retiring early allowed stand-by non-qualifiers to put in an appearance in the final. Twelve mice ran in all.

As the mice took their turns to run, MITee's time appeared impregnable. Sterling Mouse, veteran of the 1980 contest, emerged from its plastic pail to score 93.48 seconds with bonus. To its shame, Knownaim only managed a second-run best of 103.12 while Thezeus 6 was let down by its batteries without a single successful score.

With only Thezeus 4 and Enterprise left to run, the BBC television cameras stood by to give live coverage of the final. Thezeus 4 lost its bonus, and on its second run scored 68 seconds – still not good enough to beat the visitor. As Enterprise started its run the TV presenter moved close to David Otten,

"live commentary on Prestel Clubnet"

ready to broadcast a few words from the victor. First run 68.75, still too slow. Then as the telecine ran to lead into the live coverage, Enterprise snatched victory with a score of 28.78, on a bonus run taking 34 seconds. The presenter changed tack smartly, and thrust a microphone under David Woofield's nose as Enterprise set off on an even faster run.

"Are you pleased that Enterprise beat the American mouse?"

"I would have liked to beat it by a lot more," was the dour reply.

Generous cash prizes were donated by the Institution of Electrical Engineers. David Woodfield carried off prizes of £150 and £50 for the efforts of Enterprise and Knownaim – plus of course a brass cheese trophy. Alan Dibley took the runner-up's trophy plus £100, while Nick Smith gained a rather unexpected £75. Mike Windibank's Spike was the only mouse to admit to being a novice, and carried off £50 plus the Novice trophy.

The truest novice, however, was the American MITee Mouse which as a visitor was not strictly eligible to compete in the British Finals. In addition to a special visitor's trophy, Robert Scott-Kerr awarded David Otten £100 for the splendid effort of achieving second best time.

"clearly much more work needed"

One half of the rostrum had been occupied by a large wooden contraption. This was Bill Urmenyi's entry in the Robot ping-pong contest. As the mice were cleared away, Andrew Pinder's machine came to join it in battle. This Brunel system is starting to look professional and businesslike, with pneumatic cylinders and a sturdy construction. Bill's machine flexed and whirred, but with no great control. Andrew's machine hissed and lunged, but clearly there is much more work needed.

John Marr's 'Zillian' now faced John Knight's 'Charlie' with much more chance of a rally. As the ball was launched towards Charlie, the ingenious vision system locked on, the bat followed under risp servo control, and the beam-breaker fired the bat to give an excellently playable return – all with no human intervention.

"the anglepoise mechanism also showed promise"

Sadly, Zillian found the lighting too dazzling or too dim, and failed to strike up the first rally in Robat history. Its display screen showed great ability of the vision system to lock on to a bright object and predict its path – but it preferred to track the spotlight rather than the ball. The anglepoise-like mechanism also showed promise, but failed to make the necessary contact.

Prizes of £150 and £100 were donated by the Portsmouth firm of Nautech Ltd., to help the winners on their way to the mid-September European finals at Euromicro in Venice. These were won by John Knight and John Marr, respectively.

Venice should see the contest really come alive. In addition to the four Robats seen at the IEE plus another machine by James Chidley and Derek Hall, there are at least two non-British entries. From their historic micromouse achievements the Finnish team from Tampere University promise to be a force to reckon with, while Keith Buffington is bringing a Swiss contender from Zurich's ETH Institute.

Throughout the contest, Vernon Quaintance and his colleagues had been hammering their keyboards to provide a live commentary on the Prestel Club-Spot pages. These pages had scored 400 'hits' by early evening. By the time I had staggered back to Portsmouth, the results had already been picked up by Ceefax and were featured on page 266. Electronic publishing might really be getting somewhere! PE

INDUSTRY NOTEBOOK

Financial performances and gadgets galore!

REPORT BY TOM IVAL – PEs NEXUS

1986 was Industry Year but it seems that, with the exception of the electronics sector, we were not too industrious.

AS THE eminently forgettable 1986 Industry Year gently fades into obscurity the electronics sector can at least take some comfort from the fact that its financial performance will not look too bad against the general background of UK manufacturing. During the year some of the biggest companies in this field reported rather poor results relative to their 1984/85 figures.

At GEC, for example, electronics was mainly responsible for a 3.3% fall in pre-tax profits to £701 million in the year ending last March. Ferranti, which is now almost wholly an electronics company, experienced the larger drop of 11% to £41 million pre-tax profit over the same period.

Mainly because of the Inmos losses I mentioned in the October issue, Thorn-EMI's pre-tax profit was down 3.3% to £104.7 million. Subsumed in this result is some £200 million brought in from the sale of unprofitable businesses. Investment in cellular radio manufacturing and problems in data communications sales brought the Racal pre-tax profit down by 31% to £90.21 million.

But the picture was not uniformly gloomy. Down among the medium-sized companies, for instance, Oxford Instruments reported a massive 88% jump in pre-tax profits to £17.2 million on the relatively small turnover of £76 million. It's nice to know that helping people through medical instrumentation can be healthy for business as well.

Curiously, two of the oldest and best known names in British electronics are Italian: Marconi and Ferranti. Whether it's something to do with the alleged volatility of the Italian temperament I don't know, but both have experienced financial misadventures and business scandals not in keeping with traditional British phlegm.

Marconi, founded by the brilliant but odd Guglielmo of that name, who carried a sword-stick and belonged to the Italian Fascist Party, had severe financial troubles in its early years. There was also the notorious 'Marconi Scandal' of 1912 concerning alleged corruption of government ministers and price rigging of the company's shares.

Marconi was taken over by GEC and is now the most profitable of GEC's businesses with a turnover of about £1.5 billion, mostly from military electronics manufacturing.

Ferranti, though its turnover is somewhat smaller at about £600 million, is also a big wheel in UK military electronics. Currently, 31% of its turnover and 45% of its operating profit come from military equipment. Of 60 commercial announcements made over the past few months, 25 were in this field.

The other big earner for Ferranti – 38% of both turnover and profit – is computer systems, in which the company has been a great pioneer. The first Ferranti digital computer, Mark I, appeared about 25 years ago, a development from Manchester University's computer research in the 1950s. The turnover and profit figures seem to indicate that it is easier to make a profit from military electronics than from computer systems – perhaps because of the notorious 'cost plus' system I discussed in the July issue.

Ferranti was founded in the late 19th century by the pioneering electrical enginer Sebastian de Ferranti and at first was largely in power generation and transmission. For most of its life it has been a family business and even today it has a member of that family, Basil de Ferranti, as chairman of the board. Under Vincent de Ferranti, who was interested in radio, the firm started to make components for radio and television sets. Then the power transformer and electricity meter businesses were sold off to leave the company principally in electronics and related electromechanical engineering.

In this case the scandal was connected with guided missile equipment the company was producing for the Ministry of Defence. They were accused of making too much profit out of this business and, as it was public money involved, they had to pay back some of it. This did not help the company's finances and eventually, for a variety of reasons, it went bust. But because Ferranti's technological and human resources were valuable to this country it was rescued by the old National Enterprise Board (the same that started Inmos), which bought a majority shareholding. Today it is a well managed public company with shares quoted on the Stock Exchange and an apparently stable future.

Despite high unemployment in the UK, average wages are rising faster than inflation. So many people have a good deal of disposable income. Much of this has been picked up by retailers of electrical and electronics goods, helped enthusiastically by the money lenders. Indeed this boom in personal consumption has been mainly responsible for recent economic growth in the UK.

In consumer electronics there is now a tremendous variety of toys and trinkets available in the shops, quite apart from the standard domestic radio/television/hi-fi-/video recording equipment. We have had digital watches (now somewhat *déclassé*), pocket calculators, home computers, and car, camera and washing-machine control systems for many years. But now, I see, you can also buy such electronics-based novelties as a pedometer for jogging, a wrist-band pulse monitor, a nerve stimulator for muscle pains, an infra-red triggered sentry light, an acidity tester for wine-making and a key-ring which bleeps when you whistle to it (see our Christmas Offer) so that you can find it when it's lost. This is not all.

There is a wrist-band information store, a digital clock powered electro-chemically by plants, fruit or soft drinks, and an alarm-clock which stops ringing when you shout at it from your bed, not to mention a whole range of domestic special-purpose calculators and computers.

Some years ago I remember a director of Intel haranguing an audience of consumer electronics manufacturers at a conference. He maintained it was their duty to use a lot of chips in their products in order to keep the semiconductor firms in business. The message must have got home, particularly in the Far East. Many of the resulting products are trivial or bizarre, but when all the junk has disappeared I suspect there may be a residue of genuinely useful artefacts to help us in our daily lives. PE

INGENUITY UNLIMITED

Two-Type Charger

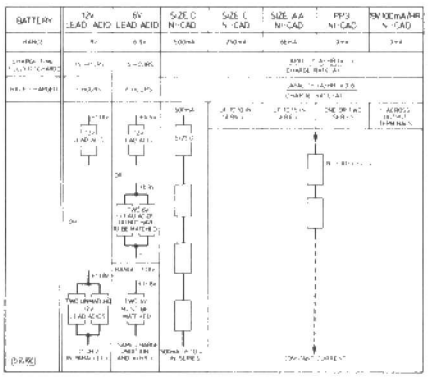
THIS circuit is for a battery charger, to charge both lead acid and nickel-cadmium type rechargeable cells. There are many types available for one type or the other but I have never seen one for both before.

The charger incorporates no metering to keep its cost down but the six l.e.d.s which show the position of the range switch are dimmed if the battery is not connected, for example there is a loose connection of the battery. This prevents hours of charging time from being wasted.

This charger is not very efficient as lots of heat must be dissipated sometimes, but such small amounts of electricity are usually not noticeable on an electricity bill. To use the charger, the correct range indicated by the relevant l.e.d, the required charging time, method of connection, maximum number of cells to be charged and range for each common battery type is shown in the table.

When switched to one of the lead acid ranges, 13.8V and 6.9V one of these voltages is present at the 741's non-inverting input and the output voltage is present at the inverting input. If the output voltage is too high then the output of the 741 goes low. The emitter follower arrangement reduces the output voltage. The opposite happens if the output voltage is too low, so the voltage at the output remains constant at the desired voltage. The zener diode produces the reference voltage which is with respect to the battery's negative terminal and not 0V.

The constant current for charging ni-cad cells is produced through the 33 ohm resistor for D, C and AA cells and through the 240 ohm resistor for PP3 cells. Under a constant current these



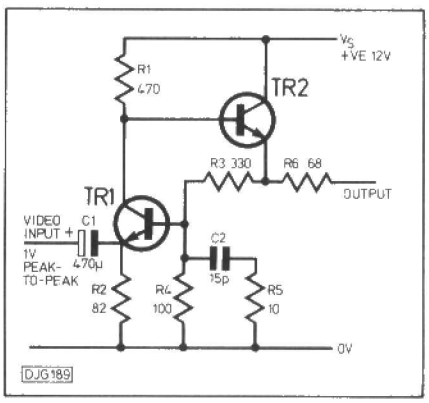
resistors have a constant voltage which is kept at the desired level as for the lead acid ranges.

In order to show that the batteries are connected, another op-amp senses the negative output terminals voltage. When a battery is connected this voltage is usually above the 0.1V produced at the non-inverting input of the op-amp so its output voltage is low making the current through the l.e.d.s around 14mA – brighter than if the battery were not connected and the op-amps output were high. On a lead acid range if the battery is almost fully charged, and the current charging it is less than 7mn, the l.e.d. dims since the potential across the 15 ohm resistor is below 0.1V. This could be an indication that the battery is fully charged but if there is any ambiguity then the battery can be disconnected for 30 seconds and then reconnected. The current surge which happens when a lead acid battery is first connected should briefly light the l.e.d.

D.E.

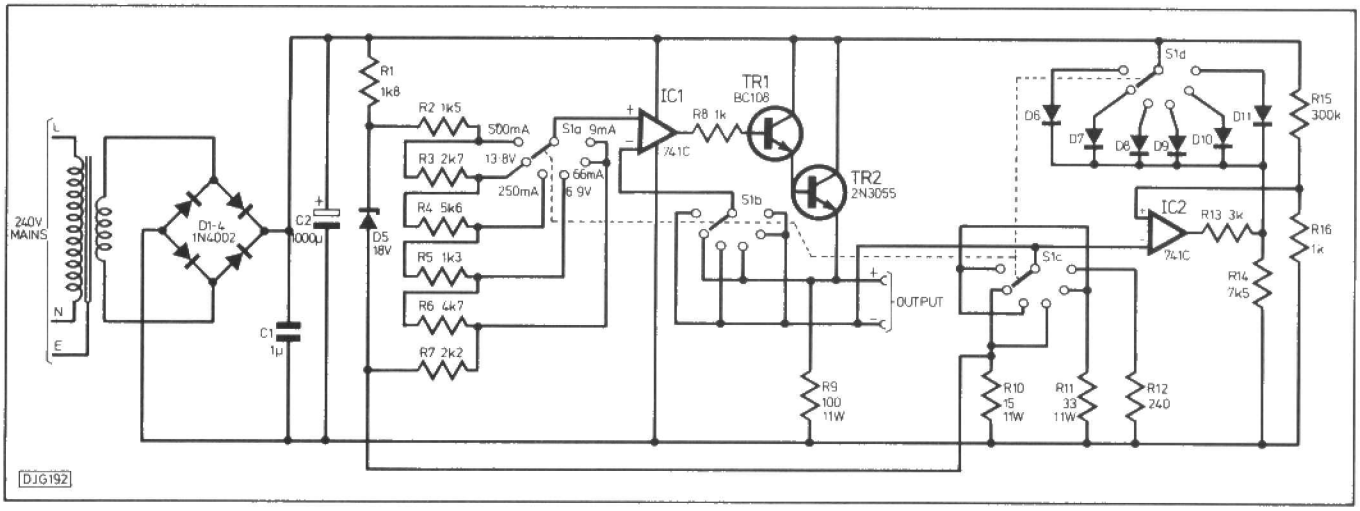
Low-Cost High Performance Video Amp

THE circuit shown in Fig. 1 is an unusual type of simple, very-wide bandwidth non-inverting video amplifier. It uses standard low cost components and exhibits a bandwidth of 5Hz to better than 75MHz without the need for expensive RF transistors and has a 75 ohm input and output impedance. TR1 whilst configured for grounded base operation actually has a relatively higher than normal input impedance due to the negative feedback applied from the output to its base, R2 alone then virutally sets the input impedance. TR2 is an output emitter follower buffer and gives the circuit a suitably low output impedance necessary for matching into 75 ohm coaxial cable.



The closed loop gain is set around 4 times by the radio of (R3+R4) / R4, C1 sets the lower frequency limit and C2 acts as the video compensation capacitor, the time constant of C2 and R4 should match that of R1 and the total stray capacitance seen at TR1 collector in order to preserve the upper frequency response. This will obviously need a small adjustment depending upon the style of layout adopted. R5 is included to avoid instability in the feedback loop since at very high frequencies the switching delays of each transistor turn the feedback positive creating a VHF phase shift oscillator.

L.S.



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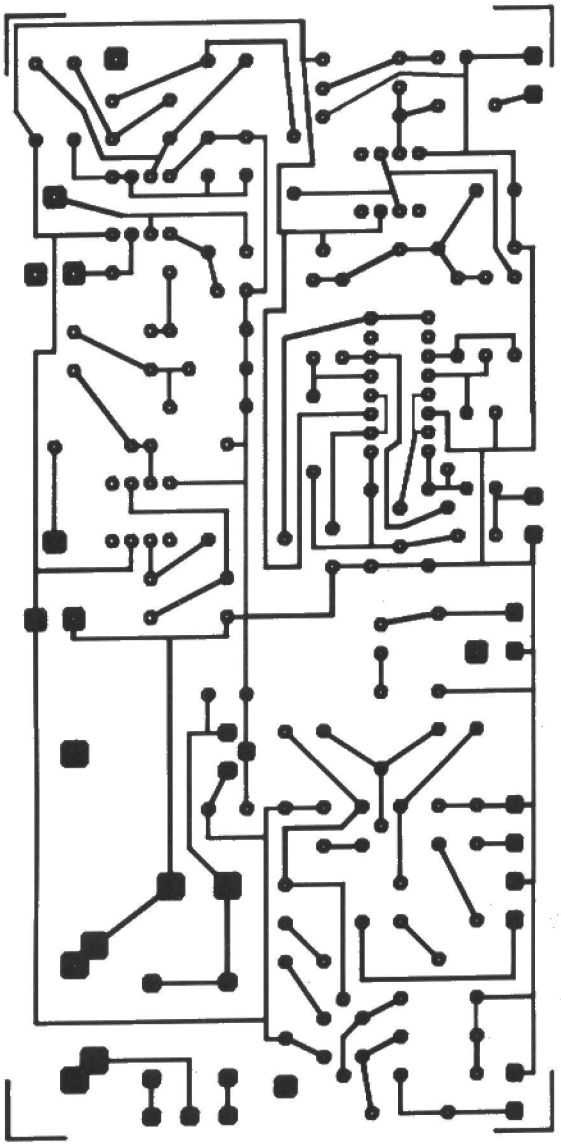

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